Reg. No._____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

THIRD SEMESTER B.TECH DEGREE EXAMINATION, JANUARY 2017

Course Code**: CS203**

Course Name**: SWITCHING THEORY AND LOGIC DESIGN (CS)**

Max. Marks: 100 Duration: 3 Hours

PART A

(Answer All Questions)

1. Convert the following numbers from the given base to the bases indicated
   a) $(250.55)_{10}$ to Hexadecimal (1)
   b) $(357)_8$ to Decimal (1)
   c) $(110101.1011)_2$ to Octal (1)
2. a) Find the 9's and 10's complement of $(13579)_{10}$ (1)
   b) Subtract $(1101)_2$ from $(11010)_2$ using i) 2's complement ii) 1's complement (2)
3. Prove the given Boolean identity using laws of Boolean algebra
   $x+x'y = x+y$ (3)
4. a) Express the given function in sum of minterms form
   $F(x, y, z) = 1$ (1½)
   b) Find the complement of the given Boolean function using De Morgan's theorem
   $F(x,y,z) = x(y'+z)$ (1½)

PART B

(Answer Any Two Questions)

5. a) What is the difference between canonical form and standard form? Which form is preferable while implementing a Boolean function with gates? (2)
   b) Simplify the given Boolean function $F(w, x, y, z) = \sum(2, 3, 12, 13, 14, 15)$
   i) Sum of Products and ii) Product of Sums (use K Map) (7)
6. a) Explain the format of single precision floating point number representation and find the decimal value corresponding to the given floating point number
   $(11000001011110110000000000000000)_2$ (4)
   b) Convert the decimal numbers 596 and 386 into BCD and do the addition and subtraction operations in BCD arithmetic. (3)
   c) What is an alphanumeric code? Why it is useful in digital computers? (2)
7. a) Express the following Boolean function in canonical form
   $F(x, y, z) = x'+yz+xz'+xy'z'+xyz'$ (3)

b) Simplify the Boolean function F (w, x, y, z) = ∑m(0, 5, 7, 8, 9, 10, 11, 14, 15) using Quine-McCluskey method. (6)

PART C

(Answer All Questions)

8. Differentiate between combinational and sequential circuits. (3)
9. Implement the Exclusive OR operation using NAND gates only. (3)
10. Give the excitation table of T Flip Flop. (3)
11. What is *state diagram*? Write down two advantages of state reduction technique. (3)

PART D

(Answer Any Two Questions)

12. a) What is the disadvantage of binary parallel adder? (2)

    b) Draw and explain the logic circuit of 4 bit full adder with look ahead carry. (7)
13. a) Explain the working of JK Flipflop. What is race around condition? How is it overcome? (4)

    b) Implement JK Flip Flop using D Flip Flop. (5)
14. a) Implement a full adder circuit using a 3×8 decoder (additional gates can be used). (5)

    b) Explain clocked sequential circuits with an example. (4)

PART E

(Answer Any Four Questions)

15. a) What is a Universal shift register? (2)

    b) Explain how a shift register is used as a converter from i) serial to parallel data and ii) parallel to serial data (8)
16. a) How does ripple counter differ from synchronous counter? (3)

    b) Design a synchronous counter with the following repeated binary sequence 000, 100, 111, 010, 011 using T Flip Flops. (7)
17. a) Compare RAM and ROM. (3)

    b) Implement the following Boolean functions using a 3×4×2 PLA

    $F1 = \Sigma (0, 1, 3, 4)$

    $F2 = \Sigma (1, 2, 3, 4, 5)$ (7)
18. Draw the block diagram of a 4 -bit ripple counter. Sketch the waveform at the output of each Flip Flop. Explain how this wave form is obtained. By what number N does this system divide? (10)
19. Write an HDL code for a full adder in all three modelling styles. (10)
20. Explain the algorithm for floating point subtraction. (10)

C **B3C037S** **Pages: 2**

Reg. No._____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

THIRD SEMESTER B.TECH DEGREE EXAMINATION, JULY 2017

CS203: SWITCHING THEORY AND LOGIC DESIGN (CS)

Max. Marks: 100 Time: 3 Hours.

PART A

Answer all questions. Each carries 3 marks.

1. Convert the following decimal numbers to binary a) 12.0625 (b) 673.23.
2. Simplify the Boolean function ***(x+y) (x+y')*** to a minimum number of literals.
3. Obtain the 1's and 2's complements for the following binary numbers: (a) 1010101 (b)0000001
4. Prove using the Boolean algebraic theorems that $x + xy = x$.

PART B

Answer any two questions. Each carries 9 marks.

5. a) Write notes on the different precision schemes used for floating point number representation. (4)

   b) Design a digital circuit with 3 inputs such that the output is equal to 1 if the majority of inputs are equal to 1. The output is 0 otherwise. Derive the truth table and obtain the simplified Boolean expressions. (5)
6. Simplify the following Boolean function by means of tabulation method.

   $F(w,x,y,z) = \sum (1,4,6,7,8,9,10,11,15)$
7. a) Describe the different schemes for representing negative numbers in binary with proper examples. (5)

   b) Perform the subtraction of following binary numbers using 2's complement representation. (i) 11010 – 10000 (ii) 100 – 110000 (4)

PART C

Answer all questions. Each carries 3 marks.

8. Give the design and circuit for a half adder.
9. Differentiate between edge triggered and level triggered flip flops.
10. Show how an XOR gate is implemented using NAND gates only.
11. What is meant by race condition in a flip flop?

PART D

Answer any two questions. Each carries 9 marks.

12. a) Describe the design and function table for a 4 to 1 line multiplexer. (5)
    b) Draw the circuit and explain the working of Master Slave JK flip flop. (4)
13. Design a code converter for converting BCD to Excess 3 code. (Circuit not required).
14. Explain how clocked sequential circuits can be designed with state equations, using an example.

PART E

Answer any four questions. Each carries 10 marks.

15. Design and implement a 4 bit binary synchronous up counter.
16. Design a Johnson counter and explain its working.
17. Draw and explain the flow chart for addition and subtraction of two binary numbers in sign magnitude form.
18. Describe the working of Programmable Logic Array (PLA) with a block diagram and a simple example.
19. a) Write notes on Read Only Memory. (5)
    b) Explain how shift registers can be used for serial transfer. (5)
20. a) Give the logic circuit for a BCD ripple counter. (5)
    b) Write notes on Random Access Memory. (5)

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Total Pages: 2

Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

THIRD SEMESTER B.TECH DEGREE EXAMINATION, DECEMBER 2017

Course Code: CS203

Course Name: SWITCHING THEORY AND LOGIC DESIGN (CS)

Max. Marks: 100 Duration: 3 Hours

PART A

Answer all questions, each carries 3 marks. Marks

1	a)	Represent +51 and -51 in 1's complement and 2's complement form.	(2)
	b)	Convert decimal $(378.93)_{10}$ to octal.	(1)
2		Perform the following decimal operations in the 8421 BCD code a) $(518)_{10} + (488)_{10}$ b) $(518)_{10} - (488)_{10}$	(3)
3		Express the following function as sum of minterms and product of maxterms: a) $F(A,B,C)=\bar{B} + A\bar{C} + A\bar{B}\bar{C}$ b) $F(A,B,C)=C(A + \bar{B})(\bar{A} + \bar{B} + \bar{C})$	(3)
4	a)	Find complement of function. $F=A\bar{B} + B\bar{C} + \bar{A}C$	(2)
	b)	Prove $AB + \bar{A}C = (A + C)(\bar{A} + B)$	(1)

PART B

Answer any two full questions, each carries 9 marks.

5	a)	Write the format of single precision floating point binary numbers. Convert the decimal number 3.248×10^4 to a single-precision floating-point binary number.	(5)
	b)	Perform the following hexadecimal operations 1) $A5C4_{16} + 39A5_{16}$ 2) $A96B_{16} - 9F2C_{16}$	(4)
6		Reduce the following expressions using K-map and implement the real minimal expression in universal logic. 1) $F(A,B,C,D)=\sum m(0,1,2,3,5,7,8,9,10,12,13)$ 2) $F(A,B,C,D)=\prod M\ (2,8,9,10,11,12,14)$	(9)
7	a)	Simplify the Boolean function $F(A,B,C,D)=\sum m(1,3,4,5,10,12,13,15)$ using Quine-McCluskey method.	(9)

PART C

Answer all questions, each carries 3 marks.

8	Differentiate between combinational and sequential circuits.	(3)
9	Draw the logic diagram of 4×1 MUX and list down the applications of MUX.	(3)
10	Give the truth table, characteristics table, excitation table and characteristic equation of SR flip-flop.	(3)
11	Compare Synchronous and Asynchronous sequential circuits.	(3)

PART D

Answer any two full questions, each carries 9 marks.

12	a)	Design a 4-bit Binary to Gray code converter.	(7)
	b)	Implement the logic function $F = A \oplus B \oplus C$ using a 8:1 multiplexer.	(2)
13	a)	Explain race around condition in JK flip-flop. Explain how a master slave flip-flop avoids race around condition.	(6)
	b)	Convert JK Flip-Flop to T Flip-Flop.	(3)
14	a)	Design and implement full subtractor by using only NAND gates.	(5)
	b)	Explain 2 bit magnitude comparator using logic diagram.	(4)

PART E

Answer any four full questions, each carries 10 marks.

15		Design a synchronous counter using JK flip-flop which counts through the states 0,1,3,4,5,6,0…… Is the counter self starting?	(10)
16		Draw and explain 4 bit Johnson counter. Also draw its timing sequence.	(10)
17	a)	Draw and explain the different types of shift registers.	(8)
	b)	List down the applications of shift registers.	(2)
18	a)	Write short notes on PLA.	(3)
	b)	Give any 2 applications of ROM.	(3)
	c)	Compare Static RAM and Dynamic RAM.	(4)
19		Find the minimum size of PLA required to implement the following functions? Hence implement the following function using PLA. $F_1(A,B,C) = \sum m(0,2,4,7)$ $F_2(A,B,C) = \sum m(3,5,6,7)$	(10)
20		Explain the algorithm for floating point addition and subtraction.	(10)

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Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

THIRD SEMESTER B.TECH DEGREE EXAMINATION, APRIL 2018

Course Code: CS203

Course Name: SWITCHING THEORY AND LOGIC DESIGN

Max. Marks: 100 Duration: 3 Hours

PART A

Answer all questions, each carries 3 marks Marks

1 Perform the following operations: (3)
i) $(E39)_{16} + (3F9)_{16}$ ii) $(721)_8 - (32)_8$
iii) BCD addition of 0110 0111 and 0101 0011

2 Perform the following conversions: (Show the steps of conversion) (3)
i) $(463.25)_{10}$ to binary ii) $(36.25)_{10}$ to octal iii) $(AF9.0C)_{16}$ to binary

3 Using Boolean postulates simplify the following expressions: (3)
i) x+x'y ii) xy+x'z+yz iii) x'y'z+x'yz+xy'

4 Express the following functions: (3)
i) F_1=AB+B'C in sum of Minterms form.
ii) F_2=A+B'C in product of Maxterms form.

PART B

Answer any two full questions, each carries 9 marks

5 Perform subtraction of the following using r's complement and (r-1)'s complement methods: (9)
i) $(7235)_{10}$- $(346)_{10}$ ii) $(1000100)_2$- $(1110100)_2$

6 Given F(A, B,C,D)= ∑(1, 4, 6, 7, 8, 9, 10, 11, 15). Simplify using Quin-McClusky method and determine the prime implicants, essential prime implicants and the minimized Boolean expression. (9)

7 a) Using K-map, simplify the Boolean function F in sum of products form, using the don't care conditions d: (5)
F(w, x, y, z) = w' (x'y + x'y' + xyz) + x'z'(y+w)
d(w, x, y, z)= w'x (y'z + yz') + wyz

b) Give the IEEE Single precision format for floating point number representation with explanation. Determine the floating-point binary number represented by the following single precision floating point representation. (4)
"1100 1010 1100 0111 0001 0000 0011 1011"

PART C

Answer all questions, each carries 3 marks

8 Implement F= A(B+CD) +B'C with NAND gates. (3)

9 Derive the simplified Boolean output functions of a full subtractor. (3)

10 Explain the terms: (3)
i) Race-around condition ii) Edge triggering of flip-flops

11		Implement D flip- flop using NAND gates and explain its working.	(3)

PART D

Answer any two full questions, each carries 9 marks

12	a)	Implement a 4- bit magnitude comparator. Give a Boolean function to check the equality relation of a pair of bits and derive logic functions for the outputs of the magnitude comparator.	(5)
	b)	Give the characteristic table and excitation table of RS flip-flop and JK flip flop.	(4)
13	a)	Implement the function with a multiplexer: $F(A, B,C,D) = \sum (0, 1, 3, 4, 8, 9, 15)$	(5)
	b)	Explain state table and state diagram with an example.	(4)
14	a)	What is a Master-slave flip-flop? Explain its working with a timing diagram.	(4)
	b)	How can the principle of look- ahead carry reduce the carry propagation time in a binary parallel adder? Derive the Boolean functions for the carry outputs at different stages of a look-ahead carry generator.	(6)

PART E

Answer any four full questions, each carries 10 marks

15		Design a BCD ripple counter. Also verify its operation by means of a timing diagram.	(10)
16	a)	Explain PLA with a block diagram.	(4)
	b)	Design a counter that has a repeated sequence of the following six states: 000, 001, 010, 100, 101, 110	(6)
17	a)	Explain the various types of ROMs	(4)
	b)	Implement a 4- bit bidirectional shift register with parallel load.	(6)
18	a)	Sketch the block diagram of a BCD adder. Using a truth table derive the condition for correction in BCD addition.	(5)
	b)	Design a serial adder using a full adder and shift registers.	(5)
19	a)	Explain the construction of a 32 X 4 ROM with a logic diagram.	(5)
	b)	Give the logical configuration of shift registers. With a block diagram, explain the use of shift registers for serial transfer of data.	(5)
20		Draw a flow chart and explain the addition/ subtraction of two binary numbers in signed magnitude representation.	(10)

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Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

THIRD SEMESTER B.TECH DEGREE EXAMINATION, DECEMBER 2018

Course Code: CS203

Course Name: SWITCHING THEORY AND LOGIC DESIGN (CS)

Max. Marks: 100 Duration: 3 Hours

PART A

Answer all questions, each carries 3 marks. Marks

1 Find the 9's and 10's complement of $(24579.12)_{10}$. (3)

2 Convert $(455)_{10}$ to base-4,8 and 16. (3)

3 Express the following functions as product of max-terms: (3)

a) F(X,Y,Z) = Y' +XZ' + XY'Z' b) F(A,B,C) = C (A+B') (A' +B' + C')

4 Use Boolean Algebra to show that A'BC'+AB'C'+AB'C+ABC'+ ABC = A+BC' (3)

PART B

Answer any two full questions, each carries 9 marks.

5 Simplify F(A,B,C,D)=Σ(1,4,6,7,8,9,10,11,15) using Tabulation method and determine the prime implicants, essential prime implicants and the minimized Boolean expression. (9)

6 a) Subtract $(9F2C)_{16}$ from $(A96B)_{16}$ using 15's and 16's complement method. (4)

b) Subtract 366 from 170 in BCD using 10's complement addition. (3)

c) Perform $(417)_8 - (232)_8$ using *8's complement addition*. (2)

7 a) Using K-map simplify the Boolean function F as Sum of Products using the don't care conditions d. (4)

F(w,x,y,z)=w'(x'y+ x'y' +xyz) + x'z'(y+w)

d(w,x,y,z)=w'x(y'z + yz) +wyz

b) Represent the following decimal numbers in signed 2's complement 8-bit numbers: i) +43 ii) –19 (3)

c) Convert the decimal number 3.248 x 10^4 to IEEE 754 standard single precision floating point binary number. (2)

PART C

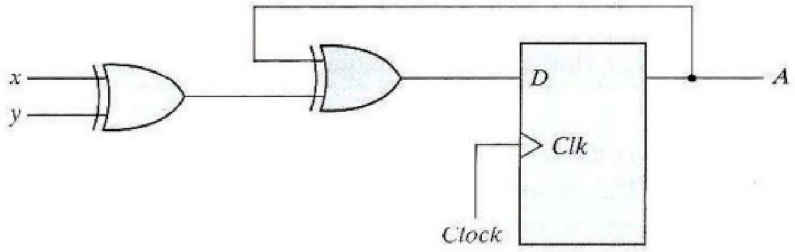
Answer all questions, each carries 3 marks.

8 Differentiate combinational and sequential circuits. (3)

9 Given the block diagram of half-subtractor, implement a full-subtractor using half-subtractors. (3)

10 Write the excitation tables of SR, JK and T flip-flops. (3)

11 Given below is a sequential circuit using D flip-flop. Write the state table and draw a state diagram. (3)



PART D

Answer any two full questions, each carries 9 marks.

12 a) Design a sequential circuit with JK Flip flops to satisfy the following state equation. (5)
A(t+1)=A'B'CD + A'B'C + ACD + AC'D' B(t+1)= A'C + CD' + A'BC'
C(t+1)= B D(t+1)=D'

b) Design and implement a decoder that decodes BCD digits (0000 to 1001). (4)

13 a) Design and implement a 2-bit magnitude comparator using 4X16 decoder. (5)

b) Implement f(A,B,C,D)= Σ(0,2,3,6,8,9,13,14) using 8 x 1 MUX . (4)

14 What is race around condition? Why does it occur? Discuss how master-slave flip-flop eliminates it. (9)

PART E

Answer any four full questions, each carries 10 marks.

15 a) Draw the logic diagram of a 4-bit Johnson counter and explain the working with a timing diagram. (8)

b) Compare Ring counter and Johnson counter. (2)

16 a) Explain the working of 3-bit *Universal* Shift Register. (8)

b) Give 2 applications of shift register. (2)

17 a) Design a combinational circuit using ROM that accepts a 3-bit binary number and generates output equal to the square of the input number. Use decoder of suitable size to implement ROM. (7)

b) What size of ROM would it take to implement (3)
i. A BCD adder/subtractor with a control input to select between the addition and subtraction.
ii. A binary multiplier that multiplies two 4-bit numbers.
iii. Dual 4-line to 1-line multiplexers with common selection inputs.

18 Design a synchronous counter using JK flip-flops to count the sequence 0,5,6,7,3,2 and then repeats. (10)

19 a) Compare static and dynamic RAMs. (3)

b) A combinational circuit is defined by the functions: (7)
F1(A,B,C)=Σ(3,5,6,7) F2= Σ(0,2,4,7)
Implement the circuit with a PLA having 3 inputs, four product terms and 2 outputs.

20 With the help of a flowchart explain the addition/subtraction of binary numbers in sign magnitude form. (10)

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Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

THIRD SEMESTER B.TECH DEGREE EXAMINATION(S), MAY 2019

Course Code: CS203

Course Name: SWITHCING THEORY AND LOGIC DESIGN

Max. Marks: 100 Duration: 3 Hours

PART A

Answer all questions, each carries 3 marks. Marks

1 List out any *three* advantages of digital systems over analogue systems. (3)

2 Do the following number conversions: (3)
(i) *base-7* number 3456 to decimal (ii) *base-4* number 1213 to binary.

3 Show the *K-map* contents for the following Boolean functions : (i) F(x,y,z) = (x+y)(y+z) (ii) F(x,y.z) = Π(0,3,5,7). (3)

4 Use *De-Morgan's principle* to find the complement of A+BC'(D+EF')' (3)

PART B

Answer any two full questions, each carries9 marks.

5 a) Do the following operations: (7)
(i) Compute *1's complement* of the binary number1101.01.
(ii) Compute *8's complement* of the octal number 672.23.
(iii) Add *base-16* numbers 1FE and EF1.

b) Assume that floating point numbers are represented in the following format. The *mantissa* is represented in *sign-magnitude* form. Magnitude of mantissa is adjusted such that the Most significant bit (MSB) is 1 and the (assumed) *binary point* is to the left of MSB. (2)

Sign bit of Mantissa (1bit)	Exponent (6 bits signed-2's complement)	Mantissa (9 bits)

Represent the decimal number 6.25 in binary.

6 Use *tabulation method* to identify the *simplified Boolean expression* for the function, F(w,x,y,z) = Π (1,3,4,6,9,11,12,14). (9)

7 a) Use *algebraic manipulation* to convert,: (5)
(i) F(x,y,z) = xy+y+z into *canonical PoS*.
(ii) F(x,y,z) = (x+y+z)(x'+y+z)(x+y'+z)(x+z) into *standard PoS*.

b) Subtract the BCD number 1671 from BCD number 837 using *10's complement* addition. (4)

PART C

Answer all questions, each carries3 marks.

8 Show how a *master-slave J-K flip-flop* can be realized using NOR and AND gates. (3)

9 Write the truth table of a 4x1 de-multiplexer and show the corresponding logic diagram. (3)

10 Show how a *full-subtractor* can be implemented using a decoder. (3)

11 Realize a *half-adder* using NAND gates. (3)

PART D

Answer any two full questions, each carries 9 marks.

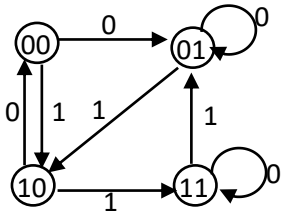
12 a) Implement the following Boolean functions using a 2X1 multiplexer and additional gates as needed: F(x,y,z) = ∑(1,2,4,5). (3)

b) Design a code converter with the following mapping specifications: (6)

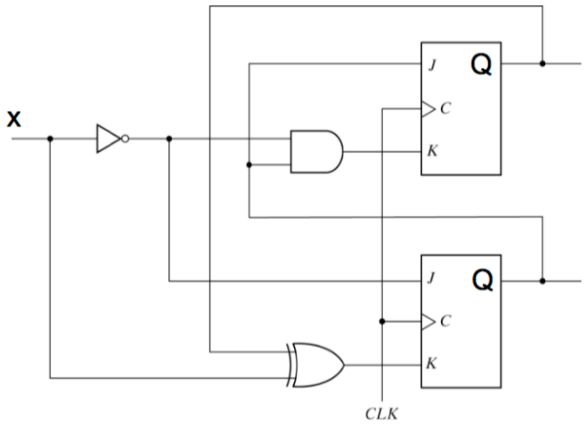
Input code	000	001	010	011	100	101	110	111
Output code	001	010	011	100	101	110	111	000

13 a) Given a 2-bit subtractor (block diagram), design a circuit with additional gates to use it as a comparator. (3)

b) Design a sequential circuit for the following *state diagram* using *T flip-flops*. (6)



14 Deduce the *state table* and *state diagram* that represents the behaviour of the following sequential circuit: (9)



PART E

Answer any four full questions, each carries10 marks.

15 With the help of a neat diagram discuss how a *serial adder* can be designed using full-adder, shift registers and flip-flop. (10)

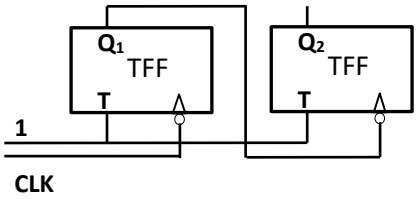
16 Design a *synchronous counter,* using edge-triggered *J-K flip-flops,* that generates the binary sequence: 001, 011, 010, 110, 111, 101, 001, 000, 001, … (10)

17 Draw a *mod-16 ripple up-counter* using J-Kflip-flops. Show how this counter can be converted to a *mod-12 ripple counter.* (10)

18 a) How is *static RAM* different from *dynamic RAM*? (3)

b) Write explanatory notes on *read-only memory* and *read-write memory*. (4)

c) Assuming that both the *T flip-flops* in the diagram below are initially at state 1, show the *timing diagram* for Q_1 and Q_2 with respect to the *falling edge* of the first *four* clock pulses. (3)



19 a) Write a short note on *PLA*. (4)

b) Implement the following Boolean functions using a *3-by-4-by-2 PLA*. (6)

(i) F1= Σ(1,4,5,6)

(ii) F2= Σ (0,2,3,4,6,7)

20 Briefly discuss the algorithms for *floating point addition* and *floating point subtraction*. (10)

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Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

THIRD SEMESTER B.TECH DEGREE EXAMINATION(R&S), DECEMBER 2019

Course Code: CS203

Course Name: SWITCHING THEORY AND LOGIC DESIGN

Max. Marks: 100 Duration: 3 Hours

PART A

Answer all questions, each carries3 marks. Marks

1		Represent decimal number $(5.75)_{10}$ in single precision floating point format.	(3)
2		Simplify the Boolean function **F= AB′+AB+BC**. Draw the circuit using basic gates. How many logic gates do you save by simplification?	(3)
3		Show the three different representations for a negative decimal number N = -25 in binary.	(3)
4		Obtain the two canonical forms of the Boolean function F(A,B,C)=**A′B+BC′+BC+AB′C′**	(3)

PART B

Answer any two full questions, each carries9 marks.

5	a)	Simplify the given Boolean function using Karnaugh Map and obtain the minimum Sum Of Products expression. F(WXYZ)=Σ(3,5,6,7)+d(10,11,12,13,14,15)	(5)
	b)	Verify or contradict the statement "NAND logic function is commutative but not associative" using truth table.	(4)
6	a)	Convert the following numbers to binary and perform subtraction both 2's complement and 1's complement. 1)Minuend $(3A)_{16}$, subtrahend $(24)_{16}$ 2)Minuend $(24)_{16}$, subtrahend $(3A)_{16}$	(5)
	b)	Obtain the simplified Product of Sums expression for the function F(ABC)=π(0,2,3,5,7) using Karnaugh Map.	(4)
7	a)	A keyboard contains 26 uppercase letters and 10 decimal digits as keys. The keys are arranged as a two-dimensional matrix. Each key should be identified by a unique binary code. Propose a suitable coding scheme for the keyboard layout. And write the code for letter H.	(5)
	b)	A digital circuit has four inputs and one output. The output is equal to 1 when (1) all the inputs are equal to 1 or (2) none of the inputs are equal to 1 or (3) an odd number of inputs are equal to 1 a) obtain the truth table b) Find the simplified output function in sum of products.	(4)

PART C

Answer all questions, each carries3 marks.

8		What is the function of a half subtractor circuit? Write the logic expression for the outputs. Draw the logic diagram of half subtractor.	(3)
9		What is the advantage of edge triggering over level triggering in flipflops?	(3)
10		Draw the diagram of a JK latch using NOR gates. Explain the working of the latch when both J and K inputs are active simultaneously.	(3)
11		Draw the schematic diagram of a 3-bit parallel adder. What is the drawback of this circuit?	(3)

PART D

Answer any two full questions, each carries9 marks.

12	a)	What is a multiplexer? Draw the internal diagram of a 4X1 multiplexer, clearly indicating the inputs and outputs. Explain the functionality using the function table	(4)
	b)	Draw the circuit of a master slave JK flipflop. With the help of a timing diagram explain its working.	(5)
13	a)	Implement the function F(A,B,C)=Σ(0,1,4,6) using a 4X1 multiplexer.	(5)
	b)	What is meant by excitation table of a flip flop? Obtain the excitation table of RS flipflop.	(4)
14	a)	Design a BCD to Excess-3 code convertor using a 4-bit parallel adder.	(5)
	b)	Draw the block diagram of a sequential circuit and differentiate synchronous and asynchronous sequential circuits.	(4)

PART E

Answer any four full questions, each carries10 marks.

15	With the help of timing diagram and logic diagram, explain the working of Serial In Serial Out shift register and Parallel In Serial Out shift register using an example.	(10)
16	Draw the logic circuit of a BCD ripple Counter and explain its working with a timing diagram	(10)
17	Show the internal architecture of a 8X4 ROM. Show the implementation of a full adder using ROM.	(10)
18	What is meant by a PLA? Show the implementation of F1=AB'C+AC+BC and F2= AC +BC+B'C using a suitable PLA.	(10)
19	Design a synchronous counter using T flipflops having states 000-001-011-101-110-111-000.	(10)
20	What is meant by Hardware Description Languages? Give examples. Write the HDL code for a 4X1 multiplexer	(10)

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Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

THIRD SEMESTER B.TECH DEGREE EXAMINATION(R&S), DECEMBER 2019

Course Code: CS203

Course Name: SWITCHING THEORY AND LOGIC DESIGN

Max. Marks: 100 Duration: 3 Hours

PART A

Answer all questions, each carries 3 marks. Marks

1 What is the largest binary number that can be expressed with 16 bits? What are the equivalent decimal and hexadecimal numbers? (3)

2 Perform subtraction on the given unsigned binary numbers using the 2's complement of the subtrahend. Where the result should be negative, find its 2's complement and affix a minus sign. (3)

(i) 10011 - 10010 (ii) 100010 - 100110

3 Find the complement of the following expressions: (3)

(i) xy' + x'y (ii) (a + c) (a + b') (a' + b + c')

4 State and Prove Absorption law in Boolean Algebra. (3)

PART B

Answer any two full questions, each carries 9 marks.

5 (a) The value of a float type variable is represented using a single precision 32 bit floating point format IEEE 754 standard that uses 1 bit for the sign , 8 bits for biased exponent and 23 bits for the mantissa. A float type variable X is assigned value of -0.0625 .What is the representation of X in hexadecimal notation? (6)

(b) Perform the following operations (3)

(i) Find the 16's complement of C3DF.

(ii) Convert C3DF to binary.

(iii) Find the 2's complement of the result in (ii)

6 (a) Add and multiply the following numbers without converting them to decimal. (6)

(i) Binary numbers 1011 and 101.

(ii) Octal numbers 62 and 37

(iii) Hexadecimal numbers 2E and 34.

(b) Represent the unsigned decimal numbers 791 and 658 in BCD, and then show the steps necessary to form their sum. (3)

7 (a) We can perform logical operations on strings of bits by considering each pair of corresponding bits separately (called bitwise operation). Given two eight- bit strings A = 10110001 and B = 10101100, evaluate the eight- bit result after the following logical operations: (3)

(i) AND (ii) OR (iii) XOR

(b) Simplify the following Boolean expressions to a minimum number of literals: (6)

(i) x'yz + xz (ii) (x + y) (x + y') (iii) xyz + x'y + xyz'

PART C

Answer all questions, each carries3 marks.

8		Design a combinational circuit with three inputs and one output. The output of the circuit is 1 when the decimal value of the inputs is less than 3. The output is 0 otherwise.	(3)
9		Implement the Boolean function **F(A, B, C, D) = π(3, 7, 12)** with a multiplexer:	(3)
10		Differentiate between Combinational and Sequential circuits. Give two examples for each.	(3)
11		Construct a JK flip-flop using a D flip-flop, a two-to-one-line multiplexer, and an inverter.	(3)

PART D

Answer any two full questions, each carries9 marks.

12	(a)	Design a four-bit 2's complementer combinational circuit. The circuit accepts a 4-bit binary number as input and generates the 2's complement of the input. Show that the circuit can be constructed with exclusive-OR gates.	(7)
	(b)	Predict what the output functions are for a five-bit 2's complementer?	(2)
13	(a)	Show that the characteristic equation for the complement output of a JK flip-flop is: $Q'(t+1) = J'Q' + KQ$	(3)
	(b)	Draw the logic diagram of a 4x16 decoder constructed with two 3x8 decoders	(4)
	(c)	Implement T flip- flop using NAND gates.	(2)
14		A sequential circuit has two JK flip-flops A and B and one input x . The circuit is described by the following flip-flop input equations: $J_A = x$ $K_A = B'$ $J_B = x$ $K_B = A$ (i) Tabulate the state table. (ii) Draw the state diagram of the circuit. (iii) Derive the state equations for A(t+1) and B(t+1)	(9)

PART E

Answer any four full questions, each carries10 marks.

15	(a)	Draw and explain the different types of shift registers.	(6)
	(b)	Explain how shift registers can be used for serial transfer.	(4)
16		Design and construct a Johnson counter with 8 distinguishable states. Give its timing diagram.	(10)
17	(a)	Design a synchronous counter with the following repeated binary sequence 000, 100,111, 010, 011 using T Flip Flops.	(6)
	(b)	Write a note on error detection and correction.	(4)
18		Find the minimum size of PLA required to implement the following functions? $F(X,Y,Z) = \Sigma m\,(1,3,5,7)$, $G(X,Y,Z) = \Sigma m\,(0,2,4,6)$	(10)
19	(a)	Design a BCD ripple counter using T flipflops	(6)
	(b)	Explain the implementation of full adder using Hardware Description Language (HDL).	(4)
20		Draw and explain the flow chart for addition and subtraction of two binary numbers in sign magnitude form.	(10)

PART E

Answer any four full questions, each carries10 marks.

15 With the help of a neat diagram discuss how a *serial adder* can be designed using full-adder, shift registers and flip-flop. (10)

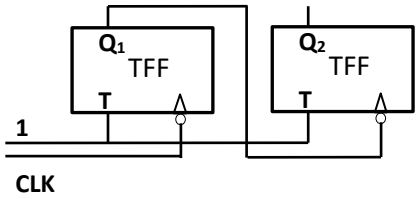
16 Design a *synchronous counter,* using edge-triggered *J-K flip-flops,* that generates the binary sequence: 001, 011, 010, 110, 111, 101, 001, 000, 001, … (10)

17 Draw a *mod-16 ripple up-counter* using J-Kflip-flops. Show how this counter can be converted to a *mod-12 ripple counter.* (10)

18 a) How is *static RAM* different from *dynamic RAM*? (3)

b) Write explanatory notes on *read-only memory* and *read-write memory*. (4)

c) Assuming that both the *T flip-flops* in the diagram below are initially at state 1, show the *timing diagram* for Q_1 and Q_2 with respect to the *falling edge* of the first *four* clock pulses. (3)



19 a) Write a short note on *PLA*. (4)

b) Implement the following Boolean functions using a *3-by-4-by-2 PLA*. (6)

(i) F1= Σ(1,4,5,6)

(ii) F2= Σ (0,2,3,4,6,7)

20 Briefly discuss the algorithms for *floating point addition* and *floating point subtraction*. (10)

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Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

Third semester B.Tech examinations (S) September 2020

Course Code: CS203

Course Name: SWITCHING THEORY AND LOGIC DESIGN

Max. Marks: 100 Duration: 3 Hours

PART A

Answer all questions, each carries 3 marks. Marks

1 (a) Express each decimal number as an 8-bit number in the 2's complement form (3)

i) +101 ii) -125

(b) Given $\sqrt{(224)_r} = (13)_r$, then what is the value of r?

2 (a) If $(73)_x = (54)_y$, then what are the possible values of x and y? (3)

(b) The 16-bit 2's complement representation of an integer is

1111 1111 1111 0101. What is its decimal representation?

3 (a) What is the result of the operation $(10111)_2 * (1110)_2$ in hexadecimal. (3)

(b) Perform $(110101)_2 - (111111)_2$ by using 2's complement method.

4 (a) Prove the Boolean identities using laws of Boolean algebra (3)

i) x+x′y = x+y ii) x+xy=x

(b) Express the following functions:

i) F1=AB+BD' in sum of Minterms form.

ii) F2=AB+B'C in product of Maxterms form.

PART B

Answer any two full questions, each carries 9 marks.

5 (a) The value of a float type variable is represented using the single-precision 32-bit floating point format IEEE-754 standard that uses 1 bit for sign, 8 bits for biased exponent and 23 bits for mantissa. A float type variable X is assigned the decimal value of −14.25. What is the representation of X in hexadecimal notation? (5)

(b) The following bit pattern represents a floating point number in IEEE 754 single precision format (4)

1 10000011 10100000000000000000000. What is the value of the number in decimal form?

6	(a)	Reduce the following expression using K-Map. AB'C+B'+BD'+ABD'+A'C	(5)
	(b)	Perform the following operations	(4)
		i. $(C45A)_{HEX}$ +$(4B26)_{HEX}$ ii. $(76)_{OCT}$ +$(23)_{OCT}$	
7	(a)	Simplify the Boolean function F (w, x, y, z) = Σm(0, 5, 7, 8, 9, 10, 11, 14, 15) using Quine-McCluskey method.	(9)

PART C

Answer all questions, each carries 3 marks.

8		Differentiate combinational and sequential circuits. Give one example for each.	(3)
9		Implement the Exclusive OR operation using NAND gates only.	(3)
10		Give the truth table, characteristics table, excitation table and characteristic equation of SR flip-flop.	(3)
11		Explain state table and state diagram with an example.	(3)

PART D

Answer any two full questions, each carries9 marks.

12	(a)	What is the disadvantage of binary parallel adder? Explain how a look ahead adder speeds up the addition process. Clearly show the derivations of equations.	(9)
13	(a)	Explain race around condition in JK flip-flop. Explain how a master slave flip flop avoids race around condition.	(6)
	(b)	Compare the working of edge-triggered flip flop and level-triggered flip flop.	(3)
14	(a)	Design a code converter for converting BCD to Excess 3 code.	(5)
	(b)	Explain the procedure to convert JK flip flop into T flip flop.	(4)

PART E

Answer any four full questions, each carries 10 marks.

15	(a)	Design and implement a 4 bit binary synchronous down counter.	(10)
16	(a)	Draw and explain 4 bit Johnson counter with its timing sequence.	(10)
17	(a)	Implement a 4- bit bidirectional shift register with parallel load.	(6)
	(b)	With a block diagram, explain the use of shift registers for serial transfer of data.	(4)
18	(a)	Describe the working of Programmable Logic Array (PLA) with a block diagram and a simple example.	(10)
19	(a)	Write notes on Read Only Memory(ROM) and give any 2 applications of ROM.	(6)
	(b)	Write notes on Random Access Memory.	(4)
20	(a)	Draw a flow chart and explain the addition / subtraction of two floating point numbers.	(10)

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