Reg. No..... Name.....

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

FOURTH SEMESTER B.TECH DEGREE EXAMINATION, JUNE 2017

Course Code**: EE 204**

Course Name**: DIGITAL ELECTRONICS AND LOGIC DESIGN (EE)**

Max. Marks: 100 Duration: 3 Hours

PART A

Answer all questions. Each question carries 5 marks

1. (a) Create a table showing 4 – bit Gray Code and the corresponding Binary Code. Explain how the table is derived. (5)
2. Using K – Map derive the reduced Boolean expression for the following function.
   $f (A , B , C , D) = \sum m (0,1,3,4,6,9,11) + d (2,5)$ (5)
3. Draw the truth table for a full subtractor. Reduce it using K – Map. Implement it using logic gates. (5)
4. Realize a J K Master Slave flip flop using NAND gates. Explain its working (5)
5. Differentiate between Asynchronouscounters and Synchronous counters with the help of diagrams. What are the advantages and disadvantages ? (5)
6. Design a 4 bit Ring counter. Draw the Truth Table and the waveform. (5)
7. Analyse the working of a R-2R ladder Digital to Analog converter with the help of a diagram. (5)
8. Design a Full Adder using VHDL. (5)

PART B

Answer any two questions. Each carries 10 marks.

9. (a) Differentiate between the methods of binary subtraction using 1's complement and 2'scomplement. Show an example in each case with 4 bit numbers. (6)
   (b) Determine the range of numbers in 1's complement and 2's compliment for word length of 8 bit and 16 bit. (4)
10. (a) Simplify using K – Map.
    $F (A , B , C , D) = \prod M (1 , 3 , 5 , 7 , 13 , 15)$ (6)
    (b) State and prove De Morgan's theorem. (4)

11. (a) Express the following function as a sum of minterms.
    $F (A , B , C ,D) = B'D + A'D + BD$ (6)
    (b) Draw the circuit diagram of a typical TTL gate and explain. (4)

PART C

Answer any two questions. Each question carries 10 marks.

12. Describe the working of a Carry Look Ahead Adder using the example of 4 – bit numbers. Clearly show the derivations of the equations. Show the implementation in Hardware. (10)
13. (a) Realize the following function using 4×1 multiplexer.
    $F(A, B, C) = \sum m(1, 3, 5, 6)$ (5)
    (b) Design a BCD to Decimal decoder. Write down the Truth Table, Boolean expressions and show the Hardware implementation. (5)
14. (a) Draw a 4 – bit Asynchronous up counter and discuss its characteristics. Draw the waveforms. (5)
    (b) Draw a 4 – bit Serial-In-Parallel-Out shift register and explain its working. (5)

PART D

Answer any two questions. Each question carries 10 marks.

15. Design a Mod 6 Synchronous counter. Enumerate all the steps in the design. (10)
16. (a) Design a two bit flash type Analog to Digital converter. Explain its working. (6)
    (b) Compare and contrast between ROM, PROM and EPROM. (4)
17. Describe the structure of a Programmable Logic Array. Take a simple example and explain. (10)

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Reg. No._____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

FOURTH SEMESTER B.TECH DEGREE EXAMINATION, JULY 2017

Course Code**: EE204**

Course Name**: DIGITAL ELECTRONICS AND LOGIC DESIGN (EE)**

Max. Marks: 100 Duration: 3 Hours

PART A

Answer all questions; each question carries 5 marks

1. Perform each of the following conversions:
   a) $(473)_{10}$ in to BCD code
   b) BAD in to ASCII
   c) $(289)_{10}$ in to hexadecimal
   d) $(110011.110)_2$ in to decimal
   e) $(53)_8$ in to hexadecimal
2. Simplify the following Boolean expression $\overline{AB} + \overline{AC} + \bar{A}\bar{B}\bar{C}$.
3. Design a half adder circuit and realize using NAND gates only.
4. Realise a JK flip flop using SR flip flop.
5. Draw the logical diagram of a 4 bit ring counter using D flip flop.
6. What are the asynchronous inputs of a flip flop and discuss its functions.
7. Compare static RAM and dynamic RAM.
8. Write the VHDL code for the implementation of a full adder circuit.

PART B

Answer any two questions; each question carries 10 marks

9. Perform arithmetic operation using 2's complement method.
   a) -70 – 85 (5)
   b) 130 – 65 (5)
10. Using a 4 variable K map, simplify,

    $F(A,B,C,D) = \sum m(1,4,9,10,11,12,14) + d(0,8,13)$

    Realize the function using NAND gates only. (10)
11. a) Describe the operation of a basic parity generating and checking logical unit. (5)

    b) Compare the characteristics of TTL and CMOS logic families. (5)

PART C

Answer any two questions; each question carries 10 marks

12. Design a MOD-12 asynchronous counter (ripple counter) using JK flip flop. Explain the working with truth table and timing diagram. (10)
13. a) Draw the block diagram of a 4 bit ALU, and explain it, showing its inputs and outputs. (5)
    b) Design a BCD to decimal decoder. (5)
14. What are fast adders? Design a 4 bit, carry look ahead adder, showing the logical diagram. (10)

PART D

Answer any two questions; each question carries 10 marks

15. Design a counter to obtain the count sequence 2, 4, 3, 6, 2, 4, 3, 6… using JK flip flop. (10)
16. a) Compare the Moore and Mealy state machine models. (5)
    b) Compare PAL and PLA. (5)
17. With a neat block schematic, describe the working of a successive approximation ADC and illustrate it with a suitable example. (10)

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Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

FOURTH SEMESTER B.TECH DEGREE EXAMINATION, APRIL 2018

Course Code: EE204

Course Name: DIGITAL ELECTRONICS AND LOGIC DESIGN (EE)

Max. Marks: 100 Duration: 3 Hours

PART A

Answer all questions, each carries 5 marks Marks

1 a) Convert the following binary number into its equivalent gray code: 11010101 (1)

b) Convert the following gray code into its binary: 10101110 (1)

c) Perform the following arithmetic operation using 2's complement representation: 58 – 34 (3)

2 Sensors are used to monitor the pressure and temperature of a chemical solution stored in a tank. The circuitry for each sensor produces a high voltage when a specified maximum value is exceeded. An alarm requiring a low voltage input must be activated when either the pressure or temperature is excessive. Design a circuit for this application. (5)

3 Draw the circuit of a full adder and explain. (5)

4 Distinguish between Sequential and combinational circuits. (5)

5 Explain the design procedure of a synchronous counter without lock out. (5)

6 Differentiate Moore and Mealy machines. Explain with examples. (5)

7 Give the basic operation of a successive approximation ADC (5)

8 Compare PAL, PLA and FPGA. (5)

PART B

Answer any two questions, each carries 10 marks

9 a) Find the standard sum of products (SOP) for the logic expression: (5)

$$F(A, B, C, D) = AB + \bar{A}B\bar{D} + B\bar{C}D$$

b) Use K-map to minimize the expression: (5)

F (A, B, C, D) =Σ m (0, 1, 2, 3, 4, 9, 10, 12, 13, 14, 15)

10 a) Design a three-bit odd parity detector circuit. (5)

b) Design the logic circuit for a BCD to decimal decoder. (5)

11 Draw a neat diagram of TTL NAND gate and explain its operation. What is meant by sourcing and sinking? (10)

PART C

Answer any two questions, each carries 10 marks

12 Explain the operation of a Master slave JK flip-flop. What is meant by race around condition? (10)

13 Design a mod-11 asynchronous counter using T flip flops and discuss its disadvantages. (10)

14 Design a 4 bit Carry look ahead adder. (10)

PART D

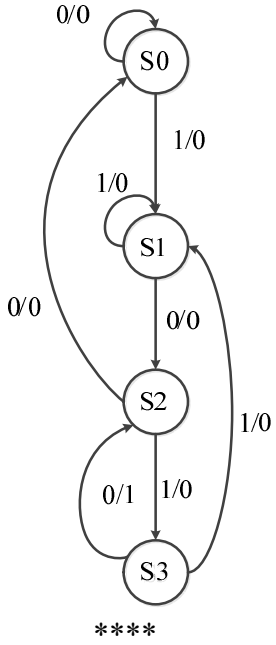
Answer any two questions, each carries 10 marks

15 Design a counter to a given count sequence using T Flip flops 1, 2, 4, 6, 0, 5, 1,..... (10)

16 Design a Flash type 2-bit ADC. What is the difficulty in designing ADCs of higher order bits? (10)

17 a) Implement a half adder using VHDL. (3)

b) Prepare the state table and excitation table for the Sequential machine shown below. Use T flip flop. (7)



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Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

FOURTH SEMESTER B.TECH DEGREE EXAMINATION, DECEMBER 2018

Course Code: EE204

Course Name: DIGITAL ELECTRONICS AND LOGIC DESIGN

Max. Marks: 100 Duration: 3 Hours

PART A

Answer all eight questions, each question carries 5 marks.

1. Why is two's - complement methodof representing signed integer numbers preferred over ones complement in digital circuits? What is range of numbers that can be represented using two complement with fourbits.
2. Expand$A + B\,\overline{C} + AB\,\overline{D} + ABCD$ to min-terms and max-terms
3. Obtain the logic function (based on the truth table) needed to implement a half adder circuit using NAND logic.
4. Explain the functioning of Master-Slave J-K flip-flop.
5. Explain the working of Johnson counter.
6. What is meant by synchronous counter? Give an example
7. What is mean by programmable logic devices?
8. Differentiate DAC and ADC

PART B

Answer any two questions, each question carries 10 marks.

9. a. With examples, explain the conversion of a gray code to corresponding binary code sequence and vice-versa. (5)
   b. Reduce the expression f= πM(0,1,2,3,4,7) using K-maps and implement it using NOR logic (5)
10. a. How parity checkers help in finding errors in digital data transmission. (5)
    b. Differentiate the features of CMOS and TTL logic gates. (5)
11. a. With examples, explain the significanceof Octal number system and Hexadecimal number system in digital circuit designs. (4)
    b. Reduce the expression f = ∑ m (0,1,2,3,5,7,8,9,10,12,13) using K-maps and implement the real minimal expression using NAND logic (6)

PART C

Answer any two questions, each question carries 10 marks.

12. What is the purpose of decoder? Explain the functioning of a BCD to Decimal Decoder circuit (10)

13. a. Differentiate Multiplexer and De-multiplexer. With simple examples, explain how they are implemented. (5)
    b. Differentiate SR and JK flip-flops. (5)
14. With the help of neat circuit and timing diagram, explain the functioning of a BCD decade asynchronous counter (MOD10) (10)

PART D

Answer any two questions, each carries 10 marks.

15. Design a counter for the following irregular binary count sequence using J-K flip flops

    001→010→101→ 111 → 001(recycles) (10)

16. a. Draw the truth-table and logic circuit diagram of a Ring counter (5)
    b. What is the basic difference between PAL (programmable Array Logic) and PLA (Programmable Logic Array). (5)
17. Explain the working of
    (i) R-2R Ladder type DAC
    (ii) Successive approximation ADC (5+5)

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Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

FOURTH SEMESTER B.TECH DEGREE EXAMINATION(R&S), MAY 2019

Course Code: EE204

Course Name: DIGITAL ELECTRONICS AND LOGIC DESIGN (EE)

Max. Marks: 100 Duration: 3 Hours

PART A

Answer all questions, each carries 5 marks Marks

1		Convert AD_{16} to its equivalent decimal and binary form.	(5)
2		Express $F = \Pi M(1,5,7)$ using SOPs and POSs and minimize the expression.	(5)
3		What is meant by race around condition? How can it be avoided?	(5)
4		Realise a full adder using the 3x8 decoder.	(5)
5		Explain Johnsons ring counter with an example.	(5)
6		What is the difference between a Moore and Mealy machines? Explain with examples?	(5)
7		Explain the working of a three-bit R-2R ladder DAC.	(5)
8		Implement $F = \Sigma m(2,3,4,5,7)$using PAL.	(5)

PART B

Answer any two questions, each carries 10 marks

9	a)	Determine the range of numbers that can be represented using signed bit, 1's complement and 2's complement form for a word length of 8 bits. Also represent and using word length of 8 bit in signed bit, 1's complement and 2's complement form.	(5)
	b)	Digital data is to be transmitted with even parity for transmitting the letter A in ASCII code. Discuss how is parity added to digital data to detect errors in transmission?	(5)
10	a)	Draw and explain the operation of TTL NAND gate.	(5)
	b)	Simplify the Boolean expression using K-map and draw the logic diagram. $F(A,B,C,D) = \sum m(0,1,5,12,13,15) + d(1,3,56)$	(5)
11	a)	Convert gray code to binary and hexadecimal.	(3)
	b)	Minimize the Boolean expression F=AB'C'+C'D+BD'+A'C using K -map and implement the logic circuit using NAND gates only.	(7)

PART C

Answer any two questions, each carries 10 marks

12 a) Realise the Boolean expression $F = \Sigma m(1,5,7,15)$ using a 4 x 1 Multiplexer (5)

b) Realise a full adder using two half adders. (5)

13 a) Discuss the different types of shift registers. (5)

b) Design a 3 bit asynchronous counter using JK flip flops. (5)

14 a) What is a glitch? Show the timing diagram for a Mod 6 asynchronous counter showing the glitches in the diagram. (5)

b) How can a 2:4 decoder be used as 1:4 Demultiplexer? (5)

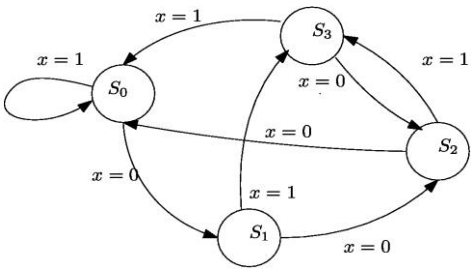
PART D

Answer any two questions, each carries 10 marks

15 a) Develop the logic circuit diagram and table for 4 -bit ring counter and explain the working. (5)

b) Explain the working of Flash type ADC. (5)

16 Develop the state diagram and design the sequential circuit using T flip flops. Also, draw the logic circuit diagram. (10)



$S_0 = 101, S_1 = 111$

$S_2 = 110, S_3 = 011$

17 a) Bring out the differences between a PAL and PLA. (4)

b) Write a VHDL program for a Full Adder (use structural approach). (6)

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Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

FOURTH SEMESTER B.TECH DEGREE EXAMINATION(S),DECEMBER 2019

Course Code: EE204

Course Name: DIGITAL ELECTRONICS AND LOGIC DESIGN

Max. Marks: 100 Duration: 3 Hours

PART A

Answer all questions, each carries 5 marks Marks

1	a)	Convert $9B30_{16}$ to decimal .	5
	b)	Subtract $5C_{16}$ from 94_{16} .	
2		Convert Y=AB + B'CD into a product of max terms by algebraic method.	5
3		Design a full subtractor and show that it can be realized using two half subtractors.	5
4		Realize an S-R flip flop using D flip flop.	5
5		What is the importance preset and clear pin in flip flops? How they are utilised when designing a counter .	5
6		Explain Moore state machine model	5
7		Draw the schematic of a successive approximation A/D converter and explain working	5
8		Differentiate ROM, PLA and PAL circuits	5

PART B

Answer any two questions, each carries 10 marks

9	a)	Explain the gray code 10110010101 to binary numbers	3
	b)	Convert 1010.011_2 into decimal number	3
	c)	Add the hexadecimal numbers $DF_{16} + AC_{16}$	4
10	a)	Differentiate the methods of binary subtraction using 1's complement and 2's complement methods with suitable example.	5
	b)	Obtain the canonical product of sum form of the following function; F(A,B,C) = (A+B')(B+C)(A+C')	5
11	a)	Apply De-Morgan's theorems to the following expression (ABC)' + (D'+E)'	5
	b)	Using karnaugh map, simplify the expression $F(A,B,C,D) = \sum (0,2,3,5,7,8,13) + d(1,6,12)$	5

PART C

Answer any two questions, each carries 10 marks

12	a)	Design a full adder circuit with decoder I C	5

	b)	Realize a 4 bit parallel binary adder with look ahead carry generator	5
13	a)	Implement the function F(A,B,C,D) =∑(0,1,3,4,8,9,15) using a suitable multiplier	5
	b)	What is the race around condition of a J-K flip flop? How can it be avoided	5
14	a)	Show how a T flip flop can be converted to S-R flip flop	5
	b)	Draw a parallel in –serial out (PISO) register and explain its working	5

PART D

Answer any two questions, each carries 10 marks

15	a)	Explain why Johnson counter have decoding gates,where as Ring counter does not?	5
	b)	Explain the design of a synchronous counter with modulus < 2^n ,take MOD -5 counter as an example to illustrate	5
16	a)	Construct a Johnson counter for 12 timing sequences.	5
	b)	Describe flash ADC and integrating type ADC	5
17	a)	Design and implement a half adder and a full adder using VHDL	5
	b)	Explain FPGA and what are the advantages of FPGA over other types of PLD	5

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Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

B.Tech S4 (S) Exam Sept 2020

Course Code: EE204

Course Name: DIGITAL ELECTRONICS AND LOGIC DESIGN (EE)

Max. Marks: 100 Duration: 3 Hours

PART A

Answer all questions, each carries 5 marks Marks

1		Convert	
	a)	$(2469)_{10}$ in to BCD.	(1)
	b)	$(735)_8$ to decimal.	(1)
	c)	$(650)_{10}$ to hexadecimal, gray and binary.	(3)
2		Using Boolean algebra prove that (A + B) (A'+C) = AC +A'B.	(5)
3		Design a full subtractor logic circuit.	(5)
4		Explain SISO and SIPO shift registers.	(5)
5		Draw the logic diagram and timing sequence of a 4-bit ring counter.	(5)
6		Prepare the state table and derive the logic expression for each flip flop input for a 3-bit binary synchronous down counter using T flip flop?	(5)
7		Explain the working of R-2R ladder type DAC.	(5)
8		Compare PAL and PLA.	(5)

PART B

Answer any two questions, each carries 10 marks

9	a)	Given X= 38_{10} and Y= 105_{10}. Using 2's complement method calculate (i) X-Y (ii) Y-X	(5)
	b)	How is the error detection and correction carried out using parity method in digital data transmission?	(5)
10	a)	Using K map, minimize the expression $F(A,B,C,D) = \sum m(1,2,3,8,14,15) + d(0,4,6,10)$.	(5)
	b)	Realize the Boolean expression Z=ABC + AD + CD' using NAND gates only.	(5)
11	a)	Explain a CMOS NAND gate .	(5)
	b)	Find the standard Product of Sum (POS) for the logic expression F=(A + B'C) C	(5)

PART C

Answer any two questions, each carries 10 marks

12 Develop a 3-stage carry look ahead adder and implement using basic gates. (10)

13 Realize the following function F(A,B,C,D) = ∑m(1,3,4,10,11,12,13) using

(i) 4 X 1 MUX (ii) 8 X 1 MUX (10)

14 a) Explain a 3 bit asynchronous up counter. Draw the timing diagram and truth table. (5)

b) Draw the logic diagram of J-K flip flop and explain it. What is the advantage of J-K flip flop over S-R flip flop. (5)

PART D

Answer any two questions, each carries 10 marks

15 Design a 3-bit gray code synchronous counter using J-K flip flop and explain the steps in detail. (10)

16 a) Compare Mealy and Moore state machine models with example. (5)

b) Differentiate between ROM and RAM. (5)

17 a) Implement a full adder circuit using VHDL (5)

b) Explain the working of successive approximation ADC. Mention the advantages and disadvantages. (5)

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