

Reg No.: _____

Name: _____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY
SEVENTH SEMESTER B.TECH DEGREE EXAMINATION, DECEMBER 2018

Course Code: CS405

Course Name: COMPUTER SYSTEM ARCHITECTURE

Max. Marks: 100

Duration: 3 Hours

PART A

Answer all questions, each carries 4 marks.

- | | | Marks |
|----|---|-------|
| 1 | With a neat sketch, explain the architecture of a vector supercomputer. | (4) |
| 2 | Explain implicit and explicit parallelism in parallel programming | (4) |
| 3 | Compare the characteristics of CISC and RISC Architectures | (4) |
| 4 | Differentiate between crossbar network and multiport memory. | (4) |
| 5 | How does cache inconsistency occur in caches due to process migration and I/O? | (4) |
| 6 | Differentiate between store and forward and wormhole routing | (4) |
| 7 | What are the possible hazards that can occur between read and write operations in an instruction pipeline? | (4) |
| 8 | Determine the frequency of the pipeline if the stage delays are $\tau_1 = 3\text{ns}$, $\tau_2 = \tau_3 = 5\text{ns}$ and $\tau_4 = 8\text{ns}$ and the latch delay is 1 ns. | (4) |
| 9 | Distinguish between static dataflow computers and dynamic dataflow computers. | (4) |
| 10 | What are the four context switching policies for multithreaded architecture? | (4) |

PART B

Answer any two full questions, each carries 9 marks.

- 11 a) Explain Flynn's classification of computer architecture (4)
- b) A 40 MHz processor was used to execute a benchmark program with the following instruction mix and clock cycle counts:

Instruction Type	Instruction count	Clock cycle count
Integer Arithmetic	35000	1
Data Transfer	20000	2
Floating point	15000	2
Control Transfer	6000	2

Determine the effective CPI, MIPS rate and execution time for this program. (5)

- 12 a) Explain the terms (i) Hit Ratio (ii) Effective Access Time with proper (3)

equations

- b) Consider the design of a three level memory hierarchy with the following specifications for memory characteristics:

Memory level	Access time	Capacity	Cost/Kbyte
Cache	$t_1=25$ ns	$s_1=512$ Kbytes	$c_1=\$1.25$
Main Memory	$t_2=903$ ns	$s_2=32$ Mbytes	$c_2=\$0.2$
Disk array	$t_3=4$ ms	$s_3=39.8$ Gbytes	$c_3=\$0.0002$

Hit ratio of cache memory is $h_1=0.98$ and a hit ratio of main memory is $h_2=0.9$.

- (i) Calculate the effective access time.
- (ii) Calculate the total memory cost. (6)
- 13 a) Explain the role of compilers in exploiting parallelism (3)
- b) Explain VLIW architecture. Also explain pipelining in VLIW processors. (6)

PART C

Answer any two full questions, each carries 9 marks.

- 14 a) Draw the state transition graph for a cache block using Goodman's write-once protocol for cache coherence. (3)
- b) Design an 8 input omega network using 2X2 switches as building blocks. (6)
Show the switch settings for the permutation $\pi_1=(0,6,4,7,3)(1,5)(2)$. Show the conflicts in switch settings, if any. Explain blocking and non-blocking networks in this context.
- 15 a) Differentiate between synchronous and asynchronous model of linear pipeline processors. (3)
- b) Consider the following pipeline reservation table:

	1	2	3	4
S1	X			X
S2		X		
S3			X	

- i) What are the forbidden latencies?
- ii) Draw the transition diagram.
- iii) List all the simple cycles and greedy cycles.
- iv) Determine the optimal constant latency cycle and minimal average latency (MAL)

- v) Let the pipeline clock period be $\tau=20\text{ns}$. Determine the throughput of the pipeline. (6)
- 16 a) Explain full-map directory based protocol. (4)
- b) What do you mean by dimension order routing? Consider a 16 node hypercube network. Based on E-cube routing algorithm, show how to route a message from 0010 to 1001. Find all intermediate nodes on routing path. (5)

PART D

Answer any two full questions, each carries 12 marks.

- 17 (a) Explain the Tomasulo's algorithm for the dynamic instruction scheduling. (5)
- (b) Explain the concept of in-order issue and out-of-order issue with respect to superscalar processor. (7)
- 18 a) Explain any three latency hiding techniques used in distributed shared memory multi computers. (9)
- b) Write a short note on fine-grain parallelism. (3)
- 19 a) Explain static branch prediction strategy and dynamic branch prediction strategy. (6)
- b) With a neat diagram explain the architecture of ETL/EM-4 dataflow architecture. (6)

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APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY
SEVENTH SEMESTER B.TECH DEGREE EXAMINATION(S), MAY 2019

Course Code: CS405

Course Name: COMPUTER SYSTEM ARCHITECTURE

Max. Marks: 100

Duration: 3 Hours

PART A

Answer all questions, each carries 4 marks.

Marks

- | | | |
|----|---|-----|
| 1 | With proper equations, explain the terms (i) CPU Time (ii) Throughput Rate | (4) |
| 2 | Explain NUMA model for Multiprocessor Systems | (4) |
| 3 | Explain the property of locality of reference in memory. | (4) |
| 4 | A generalized multiprocessor system architecture combines features from the UMA, NUMA and COMA models. Justify the answer. | (4) |
| 5 | Differentiate write-invalidate and write-update coherence protocols for write through caches. | (4) |
| 6 | Explain the factors speedup, efficiency and throughput of a k-stage linear pipeline. | (4) |
| 7 | Illustrate with example how internal data forwarding among multiple functional units can improve the throughput of a pipelined processor. | (4) |
| 8 | With an example bring out the difference between the Carry-Save Adders (CSA) and Carry Propagate Adder (CPA). | (4) |
| 9 | Explain the distributed cacheing. | (4) |
| 10 | Illustrate the scalable coherence interface (SCI) interconnect model. | (4) |

PART B

Answer any two full questions, each carries 9 marks.

- | | | |
|----|--|-----|
| 11 | a) What is the significance of Bernstein's conditions to detect parallelism? | (4) |
| | b) Consider the execution of the following code segment consisting of seven statements. Use Bernstein's conditions to detect the maximum parallelism embedded in this code. Justify the portions that can be executed in parallel and the remaining portions that must be executed sequentially. Rewrite the code using parallel constructs such as Cobegin and Coend. No variable substitution is allowed. All statements can be executed in parallel if they are declared within the same block of a (Cobegin and Coend) pair. | |

$$S1: A=B+C$$

$$S2: C=D+E$$

$$S3: F=G+E$$

$$S4: C=A+F$$

$$S5: M=G+C$$

$$S6: A=L+E$$

$$S7: A=E+A$$

(5)

12 a) Explain memory hierarchy. (3)

b) You are asked to perform capacity planning for a two-level memory system. The first level, M_1 , is a cache with three capacity choices of 64 Kbytes, 128 Kbytes, and 256 Kbytes. The second level, M_2 , is a main memory with a 4-Mbyte capacity. Let c_1 and c_2 be the cost per byte and t_1 and t_2 the access times for M_1 and M_2 respectively. Assume $c_1=20c_2$ and $t_2=10t_1$. The cache hit ratios for the three capacities are assumed to be 0.7, 0.9 and 0.98 respectively.

(i) What is the average access time t_a in terms of $t_1=20$ ns in the three cache designs? (Note that t_1 is the time from CPU to M_1 and t_2 is that from CPU to M_2)

(ii) Express the average byte cost of the entire memory hierarchy if $c_2=\$0.2/\text{Kbyte}$. (6)

13 a) Explain SIMD machine model. (3)

b) Explain Superscalar architecture. Also explain pipelining in superscalar processors. (6)

PART C

Answer any two full questions, each carries 9 marks.

14 a) Explain hot spot problem. (3)

b) Design an 8 input omega network using 2X2 switches as building blocks. Show the switch settings for the permutations $\pi_1=(0,7,6,4,2)(1,3)(5)$. Show the conflicts in switch settings, if any. Explain blocking and non-blocking networks in this context. (6)

15 a) Differentiate between linear and nonlinear pipeline processor. (3)

b) Consider the following pipeline reservation table:.

	1	2	3	4	5	6
S1	X					X
S2		X			X	
S3			X			
S4				X		
S5		X				X

- i) What are the forbidden latencies?
 - ii) Draw the transition diagram.
 - iii) List all the simple cycles and greedy cycles.
 - iv) Determine the optimal constant latency cycle and minimal average latency (MAL)
 - v) Let the pipeline clock period be $\tau=20\text{ns}$. Determine the throughput of the pipeline. (6)
- 16 a) Explain write- invalidate snoop protocol using write back policy. (4)
- b) Explain various message routing schemes used in message passing multi-computers. (5)

PART D

Answer any two full questions, each carries 12 marks.

- 17 a) Explain in detail the effect of branching and various branch handling strategies. (9)
- b) Explain the scoreboard scheme employed by the CDC 6600 processor. (3)
- 18 a) With a neat diagram explain the architecture of a multiple context processor model. (6)
- b) What are the problems of asynchrony and their solutions in massively parallel processors? (6)
- 19 a) Compare the design and performance of a superpipelined and superpipelined superscalar processors. (6)
- b) With a neat diagram explain the MIT/Motorola *T prototype multithreaded architecture. (6)

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APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY
SEVENTH SEMESTER B.TECH DEGREE EXAMINATION(R&S), DECEMBER 2019

Course Code: CS405

Course Name: COMPUTER SYSTEM ARCHITECTURE

Max. Marks: 100

Duration: 3 Hours

PART A

Answer all questions, each carries 4 marks.

- | | | Marks |
|----|--|-------|
| 1 | A 400MHz processor was used to execute a program with 150000 floating point instructions with clock cycle count of 1. Determine the execution time and MIPS rate for this program. | (4) |
| 2 | State Amdahl's law. Write an expression for the overall speed up. | (4) |
| 3 | Distinguish between scalar RISC and super-scalar RISC in terms of instruction issue, pipeline architecture and performance. | (4) |
| 4 | Discuss the schematic representation of a generalized multiprocessor system. | (4) |
| 5 | Explain chained cache coherence protocol. | (4) |
| 6 | Consider the execution of a program of 15,00,000 instructions by a linear pipeline processor with a clock rate of 1000 MHz. Assume that the instruction pipeline has five stages and that one instruction is issued per cycle. The penalties due to branch instruction and out-of-order execution are ignored. <ul style="list-style-type: none"> a) Calculate the speedup factor in using this pipeline to execute the program as compared with the use of an equivalent non-pipelined processor with an equal amount of flow-through delay. b) Find out the efficiency and throughput of this pipelined processor. | (4) |
| 7 | Write short notes on internal data forwarding. | (4) |
| 8 | Explain Goodman's write once protocol with transition diagram. | (4) |
| 9 | List any two advantages and disadvantages of Scalable Coherence Interface(SCI). | (4) |
| 10 | What are the four context switching policies adopted by multithreaded architectures? | (4) |

PART B

Answer any two full questions, each carries 9 marks.

- | | | |
|----|--|-----|
| 11 | a) Discuss the Bernstein's conditions for checking the parallelism among a set of processes. | (3) |
| | b) Analyze the data dependences among the following statements and construct a | (6) |

dependency graph. Also detect the parallelism embedded in them.

S1 : Load R1 , M(100) / R1 \leftarrow Memory(100) /

S2 : Move R2 , R1 / R2 \leftarrow (R1) /

S3 : Inc R1 / R1 \leftarrow (R1) + 1 /

S4 : Add R2 , R1 / R2 \leftarrow (R2) + (R1) /

S5 : Store M(100), R1 / Memory(100) \leftarrow (R1) /

- 12 a) Define the inclusion property of a memory hierarchy. Illustrate the data transfers between adjacent levels of a memory hierarchy. (5)
- b) Consider a two-level memory hierarchy, M1 and M2 of sizes 64Kbytes and 4Mbytes respectively, with access time $t_1 = 20\text{ns}$ and $t_2 = 200\text{ns}$ and costs c_1 and c_2 are \$0.01/byte, $c_2 = \$0.0005/\text{byte}$ respectively. The cache hit ratio $h_1 = 0.95$ at the first level. Find the effective access time and total cost of this memory system. (4)
- 13 Differentiate between the following with necessary diagrams:
- a) UMA and NUMA multiprocessor models. (4)
- b) RISC and CISC (5)

PART C

Answer any two full questions, each carries 9 marks.

- 14 a) Explain the different levels of hierarchy of bus systems. (4)
- b) Define the write-invalidate snoop bus protocol for maintaining cache coherence. Show the different possible state transitions for write-through and write-back cache using the write-invalidate protocol. (5)
- 15 Consider the five-stage pipelined processor specified by the following reservation table and answer the following: (S indicate the stages)

	1	2	3	4	5	6
S1	X					X
S2		X		X		
S3			X			
S4				X	X	

- (i) List the set of forbidden latencies and the collision vector. (2)
- (ii) Draw the state transition diagram showing all possible initial sequences without causing a collision in the pipeline. (3)

- (iii) List all the simple and greedy cycles from the state diagram. (2)
- (iv) Determine the minimal average latency (MAL). (2)
- 16 a) Explain the three major operational characteristics of a multiprocessor interconnection network. (3)
- b) Analyse and compare the communication latencies of Store-and Forward and Wormhole routing schemes. (3)
- c) Consider a 16-node hypercube network. Based on the E-cube routing algorithm, show how to route a message from node (0111) to node (1101). All intermediate nodes must be identified on the routing path. (3)

PART D

Answer any two full questions, each carries 12 marks.

- 17 a) Which are the three logic hazards possible in an instruction pipeline? Define each. Write the necessary conditions for each to occur. (6)
- b) Explain the in-order and out-of-order pipeline scheduling policies for a superscalar machine with an example. (6)
- 18 a) Explain the importance of Tomasulo's algorithm for dynamic instruction scheduling. (8)
- b) What do you mean by Release Consistency (RC) memory model? Give the conditions to ensure RC. (4)
- 19 a) Explain the effect of branching in instruction pipelining. Find the execution time and throughput of the pipeline for n instructions by considering the effect of branching. How branch penalty is reduced using delayed branch strategy. (6)
- b) Explain any two latency hiding techniques used in distributed shared memory multi computers. (6)

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

Seventh semester B.Tech examinations (S), September 2020

Course Code: CS405**Course Name: COMPUTER SYSTEM ARCHITECTURE**

Max. Marks: 100

Duration: 3 Hours

PART A*Answer all questions, each carries 4 marks.*

Marks

- | | | |
|----|---|-----|
| 1 | With neat sketch differentiate explicit and implicit parallelism. | (4) |
| 2 | Explain COMA model for Multiprocessor Systems. | (4) |
| 3 | Define a) Instruction issue latency b) Instruction issue rate. | (4) |
| 4 | Explain the significance of multiport memory. | (4) |
| 5 | How hardware synchronization can be achieved in a multiprocessor system. | (4) |
| 6 | Explain different message routing schemes. | (4) |
| 7 | What is meant by pipeline stalling? | (4) |
| 8 | Differentiate between Carry save adder (CSA) and Carry propagation adder (CPA). | (4) |
| 9 | Suggest different methods to overcome asynchrony problem. | (4) |
| 10 | Explain distributed caching. | (4) |

PART B*Answer any two full questions, each carries 9 marks.*

- | | | |
|----|---|-----|
| 11 | a) Define Amdahl's Law. | (3) |
| | b) Consider the execution of an object code with 200,000 instructions on a 40-MHz processor. The program consists of four major types of instructions. The instruction mix and the number of cycles (CPI) needed for each instruction type are given below based on the result of a program trace experiment. | (6) |

Instruction type	CPI	Instruction mix
Arithmetic and logic	1	56%
Load/store with cache hit	2	22%
Branch	4	10%
Memory reference with cache miss	8	12%

Calculate the average CPI, MIPS rate and Execution time.

- | | | |
|----|--|-----|
| 12 | a) Compare RISC and CISC scalar processor architectures. | (4) |
|----|--|-----|

- b) Consider the design of a three-level memory hierarchy with the following specifications for memory characteristics: (5)

Memory Level	Access time	Capacity	Cost/Kbyte
Cache	$t_1=20\text{ns}$	$s_1=512\text{Kbytes}$	$c_1=\$1.30$
Main Memory	$t_2=905\text{ns}$	$s_2=32\text{Mbytes}$	$c_2=\$0.2$
Disk array	$t_3=5\text{ms}$	$s_3=40\text{Gbytes}$	$c_3=\$0.0003$

Hit ratio of cache memory is $h_1=0.98$ and a hit ratio of main memory is $h_2=0.9$.

- (i) Calculate the effective access time.
- (ii) Calculate the total memory cost.
- 13 a) State and explain Bernstein's conditions for parallelism? (3)
- b) Detect parallelism in the following code using Bernstein's conditions. Assume there are sufficient numbers of resources available. (6)
- P1: $C=D * E$
- P2: $M=G+C$
- P3: $A=B+C$
- P4: $C=L+M$
- P5: $F=G/E$

PART C

Answer any two full questions, each carries 9 marks.

- 14 a) Design an 8 input omega network using 2×2 switches as building blocks. Show the switch settings for the permutation $\pi_1=(0,6,3,2,5)(1,4)$. Show the conflicts in switch settings, if any. Explain blocking and non-blocking networks in this context. (6)
- b) Draw the two state transition graphs for a cache block using write -invalidate write -through snoopy bus protocol. (3)
- 15 a) With suitable diagram explain different flow control strategies for resolving a collision between two packets. (4)
- b) Consider the following pipeline reservation table. (5)

	1	2	3	4
S1	X			
S2		X		X
S3			X	

- i) What are the forbidden latencies?
 - ii) Draw the transition diagram.
 - iii) List all the simple cycles and greedy cycles.
 - iv) Determine the optimal constant latency cycle and minimal average latency (MAL).
 - v) Let the pipeline clock period be $\tau=10\text{ns}$. Determine the throughput of the pipeline.
- 16 a) Compare full map directories with limited directories. (4)
- b) Explain E-cube routing. Consider a 64 -node hypercube network. Based on E-cube routing algorithm, show how to route a message from 101101 to 011010. Find all intermediate nodes on routing path. (5)

PART D

Answer any two full questions, each carries 12 marks.

- 17 a) Explain the importance of Tomasulo's algorithm for dynamic instruction scheduling. (6)
- b) Describe the various mechanisms for improving the performance of instruction pipeline. (6)
- 18 a) Explain various latency hiding techniques. (8)
- b) Differentiate between static and dynamic data flow computers. (4)
- 19 a) Explain various branch prediction techniques. (6)
- b) With suitable diagrams explain ETL/EM-4 architecture. (6)

Reg No.: _____

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APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

Seventh Semester B.Tech Degree Examination (Regular and Supplementary), December 2020

Course Code: CS405**Course Name: COMPUTER SYSTEM ARCHITECTURE**

Max. Marks: 100

Duration: 3 Hours

PART A*Answer all questions, each carries 4 marks.*

Marks

- 1 State Amdahl's law. Suppose that we want to enhance the processor used for a server machine. The new processor is 15 time faster on computation in the serving applications than the original processor. Assuming the original processor is busy with computation 30% and waiting for I/O 70% time, what is the overall speedup gained by incorporating the enhancement. (4)
- 2 Explain UMA model for Multiprocessor Systems. (4)
- 3 Define the inclusion property of a memory hierarchy with diagram. (4)
- 4 How does cache inconsistency occur in caches due to sharing writable data and process migration? (4)
- 5 Differentiate between synchronous and asynchronous model of linear pipeline processors. (4)
- 6 Explain different flow control strategies for resolving a collision between two packets. (4)
- 7 What is dynamic instruction scheduling? (4)
- 8 What is meant by pipeline stalling? (4)
- 9 Explain the different context switching policies adopted by multithreaded architectures. (4)
- 10 Write short notes on fine-grain parallelism. (4)

PART B*Answer any two full questions, each carries 9 marks.*

- 11 a) Explain different types of data dependence with example. (4)

- b) Consider the execution of an object code with 100,000 instructions on a 40-MHz processor. The program consists of four major types of instructions. The instruction mix and the number of cycles (CPI) needed for each instruction type are given below based on the result of a program trace experiment. (5)

Instruction type	CPI	Instruction mix
Arithmetic and logic	1	60%
Floating point Arithmetic	2	20%
Load/store	4	10%
Memory reference	6	10%

Calculate the average CPI, MIPS rate and Execution time.

- 12 a) Compare CISC and RISC machines in terms of addressing modes, instruction format and CPI. (3)
- b) Consider the design of a three-level memory hierarchy with the following specifications for memory characteristics: (6)

Memory Level	Access time	Capacity	Cost/Kbyte
Cache	$t_1 = 25 \text{ ns}$	$S_1 = 512 \text{ Kbytes}$	$C_1 = \$0.12$
Main memory	$t_2 = \text{unknown}$	$S_2 = 32 \text{ Mbytes}$	$C_2 = \$0.02$
Disk array	$t_3 = 4 \text{ ms}$	$S_3 = \text{unknown}$	$C_3 = \$0.00002$

Our aim is to achieve an effective memory-access time $t = 850 \text{ ns}$ with a cache hit ratio $h_1 = 0.98$ and a hit ratio $h_2 = 0.99$ in the main memory. Also, the total cost is upper-bounded by \$1,500. Calculate unknown specifications based on these conditions.

- 13 a) Explain Flynn's classification of computer architecture. (3)
- b) Explain pipelining in following processors. (6)
- i) Superscalar processor ii) VLIW processor iii) Vector processor

PART C

Answer any two full questions, each carries 9 marks.

- 14 a) Design an 8 input omega network using 2X2 switches as building blocks. Show the switch settings for the permutation $\pi_1=(0,5,4,7,2)(1,6)(3)$. Show the conflicts in switch settings, if any. Explain blocking and non-blocking networks in this context. (6)
- b) Explain the significance of multiport memory. (3)
- 15 a) Explain Dimension order routing with example. (4)
- b) Consider the following pipeline reservation table: (5)

	1	2	3	4	5	6
S1	X				X	
S2			X			
S3		X		X		X

- i) What are the forbidden and permissible latencies?
- ii) Draw the state transition diagram.
- iii) List all the simple cycles and greedy cycles.
- iv) Determine the minimal average latency (MAL).
- 16 a) Define Write –invalidate Snoopy Bus Protocol. Draw and explain the 2 state transition graphs for a cache block using write –invalidate write -through and write-back snoopy bus protocols. (6)
- b) Compare the communication latencies of Store-and Forward and Wormhole routing schemes. (3)

PART D

Answer any two full questions, each carries 12 marks.

- 17 a) Describe the various mechanisms for instruction pipelining. (6)
- b) Compare static and dynamic branch prediction strategies. Explain how delayed branches reduces branch penalty. (6)
- 18 a) Explain any three latency hiding techniques used in distributed shared memory multicomputers. (6)
- b) What are the problems of asynchrony and their solutions in massively parallel processors? (6)
- 19 a) Explain the concept of in-order issue and out-of-order issue with respect to superscalar processor. (6)
- b) Explain the data flow architecture. (6)
