B **B4B071** **Pages: 2**

Reg. No._____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY
FOURTH SEMESTER B.TECH DEGREE EXAMINATION, MAY 2017

CS202: COMPUTER ORGANISATION AND ARCHITECTURE (CS, IT)

Max. Marks: 100 Time: 3 hrs

PART A

Answer all questions. Each carries 3 marks.

1. Write notes on condition codes.
2. Explain indirect addressing with an example.
3. Draw the flow chart for Booth's Multiplication algorithm.
4. Explain the process of storing a word in memory using a single bus organization. Specify which all control signals will be activated.

PART B

Answer any two questions. Each carries 9 marks.

5. a) Briefly explain the memory access instructions and addressing modes of ARM processor (4)
   b) Write notes on multiple bus organization (5)
6. Explain the terms processor stack, stack frame and frame pointer with relation to subroutine processing. Use a relevant example.
7. Draw and explain the flow charts for floating point multiplication and division.

PART C

Answer all questions. Each carries 3 marks.

8. Differentiate between programmed I/O and interrupt driven I/O.
9. Define the terms a)Latency b)Bandwidth c)Memory cycle time
10. Why do dynamic RAMs need constant refreshing? How is this done?
11. Explain Direct Memory Access. What is burst mode DMA?

PART D

Answer any two questions. Each carries 9 marks.

12. a) Distinguish between centralized and distributed bus arbitration? (4)
    b) Write notes on set associative cache mapping. (5)

13. a) Distinguish between synchronous and asynchronous DRAMs (4)
    b) Explain the important Data transfer signals on the PCI bus. (5)
14. a) Describe the different types of ROMs. (4)
    b) Explain the procedure and the packets used for an output transfer in USB interface. (5)

PART E

Answer any four questions. Each carries 10 marks.

15. Describe processor organization with diagram using a) scratchpad memory b) Two port memory. (10)

16. Design a 4bit Arithmetic unit which performs the following operations on two inputs A and B, controlled by selection variables s_1 and s_0 and input carry C_{in}: (10)

s_1	s_0	$C_{in} = 0$	$C_{in} = 1$
0	0	F=A	F=A+1
0	1	F=A+B	F=A+B+1
1	0	F=A+B'	F=A+B'+1
1	1	F=A-1	F=A

17. a) Write notes on status register. (5)
    b) Distinguish between horizontal and vertical microinstructions. (5)
18. What is the significance of a micro program sequencer? Explain its working with the help of a diagram.
19. Explain micro programmed CPU organization with the help of a diagram.
20. With the help of a block diagram, describe a complete processor unit with all components and appropriate control variables. Show with an example, how a control word for the processor can be defined.

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Total Pages: 2

Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

FOURTH SEMESTER B.TECH DEGREE EXAMINATION, JULY 2017

Course Code: CS202

Course Name: COMPUTER ORGANISATION AND ARCHITECTURE (CS, IT)

Max. Marks: 100 Duration: 3 Hours

PART A

Answer all questions. Each carries 3 marks.

1		Differentiate between big-endian and little-endian byte assignments.	(3)
2		Design a 2x2 array multiplier.	(3)
3		Describe auto increment addressing mode with the help of an example.	(3)
4		Give the control sequence for execution of instruction Add[R2],R1 using a single bus organization.	(3)

PART B

Answer any two questions. Each carries 9 marks.

5	a)	Describe, with proper examples, the role of processor stack in subroutine call and return.	(5)
	b)	Draw the flowchart for decimal multiplication.	(4)
6	a)	Explain restoring method of division with the help of a flow chart.	(5)
	b)	Write notes on three address, two address and one address instructions, giving example for each.	(4)
7	a)	Explain single bus organization with the help of a diagram. Specify with examples, how memory operations are done in the given organization.	(5)
	b)	Describe any 4 addressing modes with examples.	(4)

PART C

Answer all questions. Each carries 3 marks.

8		What are vectored interrupts?	(3)
9		Write notes on flash memory.	(3)
10		Briefly explain the LRU cache replacement algorithm	(3)
11		Describe centralized bus arbitration.	(3)

PART D

Answer any two questions. Each carries 9 marks.

12	a)	Explain the architecture of USB with a diagram. What do you mean by split bus operation in USB?	(5)
	b)	Write notes on static memories.	(4)

13	a)	Differentiate between associative and set associative cache mapping with examples.	(5)
	b)	Write notes on interrupt nesting. Explain how simultaneous interrupt requests can be handled.	(4)
14	a)	Discuss about the different types of Read only memories.	(4)
	b)	Explain with the help of timing diagrams, the input and output data transfers in an asynchronous bus.	(5)

PART E

Answer any four questions. Each carries 10 marks.

15	a)	Design a bus system for interconnecting four n bit registers	(5)
	b)	Design a 4bit combinational logic shifter	(5)
16	a)	Briefly explain, with diagrams, the different methods for control organization	(5)
	b)	Write notes on microprogrammed CPU organisation.	(5)
17	a)	Design an adder/subtractor circuit with one selection variable s and two inputs A and B. When s=0, the circuit performs A+B and when s=1 it performs A-B, by taking 2's complement of B.	(5)
	b)	Write notes on status register.	(5)
18	a)	Describe the different ways in which a general-purpose processor unit can be organized.	(6)
	b)	Write notes on conditional control statements.	(4)
19		Explain with the help of a diagram, the working of microprogram sequencer.	(10)
20		Describe the steps in control logic design with the help of an example. (Example can be realised using either hardwired or microprogrammed control organization.)	(10)

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Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY
FOURTH SEMESTER B.TECH DEGREE EXAMINATION, APRIL 2018

Course Code: CS202

Course Name: COMPUTER ORGANIZATION AND ARCHITECTURE (CS, IT)

Max. Marks: 100 Duration: 3 Hours

PART A
Answer all questions, each carries 3 marks Marks

1 With a neat diagram, explain the internal architecture of the CPU. (3)

2 What are condition codes? List the different condition codes. (3)

3 Prove that the worst case delay through an $n \times n$ array multiplier is $6(n-1)-1$ gate delays. (3)

4 Enumerate the sequence of actions involved in executing an unconditional branch instruction. (3)

PART B
Answer any two questions, each carries 9 marks

5 a) With the help of examples, explain the different addressing modes. (5)

b) Register R6 is used in a program to point to the top of a stack containing 32-bit numbers. Write a sequence of instructions using the Index, Autoincrement, and Autodecrement addressing modes to perform each of the following tasks: (4)
(*a*) Pop the top two items off the stack, add them, then push the result onto the stack.
(*b*) Copy the fifth item from the top into register R3.
For each case, assume that the stack contains ten or more elements.

6 a) With the help of a diagram, describe the datapath inside the processor. (5)

b) Discuss the different ways in which the return address can be saved during a subroutine call. Which of these methods support subroutine nesting? Justify your answer. (4)

7 a) Write down the sequence of actions needed to fetch and execute the instruction: (3)

Store R6, X(R8).

b) Multiply each of the following pairs of signed 2's-complement numbers using the Booth algorithm. In each case, assume that A is the multiplicand and B is the multiplier. (6)
i) A = 001011 and B = 011011
ii) A = 000111 and B = 000111

PART C
Answer all questions, each carries 3 marks

8 Explain the functions of interface circuits. (3)

9 List and describe the registers in a DMA interface. (3)

10		The cache block size in many computers is in the range of 32 to 128 bytes. What would be the main advantages and disadvantages of making the size of cache blocks larger?	(3)
11		What is flash memory?	(3)

PART D

Answer any two questions, each carries 9 marks

12	a)	With a diagram, explain the PCI bus.	(5)
	b)	Write a note on the packet type formats of USB.	(4)
13	a)	What are interrupts? List the sequence of steps following an interrupt request.	(5)
	b)	Describe semiconductor RAM memories.	(4)
14	a)	With the help of an example, explain the different cache mapping function	(6)
	b)	A computer system has a main memory consisting of 1M 16-bit words. It also has a 4K-word cache organized in the block-set-associative manner, with 4 blocks per set and 64 words per block. Calculate the number of bits in each of the Tag, Set, and Word fields.	(3)

PART E

Answer any four questions, each carries 10 marks

15	a)	Discuss shift and conditional control micro operations.	(7)
	b)	An 8-bit register A has one input x. The register operation is represented symbolically as P: $A_7 \leftarrow x$, $A_i \leftarrow A_{i+1}$ $i = 0,1,2,3 \ldots 6$. What is the function of the register?	(3)
16		Compare vertical and horizontal microinstruction formats, giving examples.	(10)
17		With a diagram, explain how control signals are generated using hardwired control.	(10)
18		Describe the purpose of microprogram sequencing. How is it carried out?	(10)
19		Draw the block diagram for the hardware that implements the following statement x + yz: AR ← AR + BR where AR and BR are two n-bit registers and x, y, and z are control variables. Include the logic gates for the control function. (The symbol + designates an OR operation in a control or Boolean function and an arithmetic plus in a micro operation.)	(10)
20		Explain the design of status register.	(10)

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Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

FOURTH SEMESTER B.TECH DEGREE EXAMINATION, DECEMBER 2018

Course Code: CS202

Course Name: COMPUTER ORGANIZATION AND ARCHITECTURE (CS, IT)

Max. Marks: 100 Duration: 3 Hours

PART A

Answer all questions. Each carries 3 marks.

1		Write the three-address, two-address and one-address representations of the operation below with relevant assumptions: $C \leftarrow [A] + [B]$	3
2		What is the use of linkage register in subroutine invocation?	3
3		Why is non-restoring division faster than restoring division?	3
4		Design and draw a 3X2 array multiplier.	3

PART B

Answer any two questions. Each carries 9 marks.

5		Illustrate various addressing modes with proper examples. Which is the default addressing mode selected by assemblers and compilers and why?	9
6		Give the flow chart for Booth's Algorithm. Illustrate using an example.	9
7	(a)	Assuming that stack grows towards lower address range write assembly code for the following (Without using PUSH and POP) : (i) Pushing elements stored at ITEM1, ITEM2 onto stack (ii) Popping an element onto address ITEM (iii) Copying value of top of stack to address TOP	4.5
7	(b)	Compare and contrast single bus and multiple bus organisation of CPU.	4.5

PART C

Answer all questions. Each carries 3 marks.

8		Compare the two main modes of DMA transfer.	3
9		Explain any two interrupt priority schemes.	3
10		What is MFC signal? How is it related to Memory Access Time?	3
11		Which design feature of SRAM cells helps in value retention without refresh?	3

PART D

Answer any two questions. Each carries 9 marks.

12		Illustrate with an example SCSI bus arbitration and selection.	9
13		With the help of a diagram examine the internal organisation of bit cells in a memory chip.	9
14	(a)	Explain the architecture of USB with help of a diagram.	4.5
14	(b)	Differentiate Direct and Associative mapped cache with examples.	4.5

PART E

Answer any four questions. Each carries 10 marks.

15	Give a simple design for generating status bits for a 8-bit ALU.	10
16	Draw a labelled block diagram of a processor unit with seven registers R1 to R7,a status register,ALU with 3-selection variables and $C_{in,}$ and shifter with 3 selection variables.	10
17	With the help of a flowchart for sign-magnitude addition/subtraction, explain the steps involved in developing a hardwired control unit.	10
18	Using a block diagram analyse the design of a microprogram control for a processor unit.	
19	What is a control word? With the help of proper illustrations and assumptions show how a designer would compose a control word for the processor unit.	10
20	With the help of a diagram establish the functioning of microprogram sequencer in a microprogram controlled processor.	10

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Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY
FOURTH SEMESTER B.TECH DEGREE EXAMINATION(R&S), MAY 2019

Course Code: CS202

Course Name: COMPUTER ORGANISATION AND ARCHITECTURE (CS, IT)

Max. Marks: 100 Duration: 3 Hours

PART A

Answer all questions,each carries 3 marks

1		Explain one, two and three address instruction with an example for each.	3
2		List the steps involved in invoking a subroutine through the use of a link register.	3
3		Draw a 3 x 2 array multiplier.	3
4		Non-restoring division is faster than restoring division. Justify the statement.	3

PART B

Answer any two questions, each carries 9 marks

5		List various addressing modes explain any four with an example for each.	9
6	a)	Draw the diagram of a multi-bus organization with 3 buses. Write the control sequence for the instruction Add R4, R5, R6 for the above mentioned multi-bus organization.	5
	b)	Give the sequence of control steps required to perform the operation Add [R3], R1 in a single-bus organization.	4
7	a)	Divide $(1000)_2$ by $(11)_2$ using restoring division method.	4
	b)	Illustrate the basic operational concepts in transferring data between main memory and processor with neat diagram.	5

PART C

Answer all question, each carries 3 marks

8		What are vectored interrupts?	3
9		Give the functions of initiator and target controllers in SCSI bus.	3
10		Compare synchronous and asynchronous DRAM.	3
11		Define temporal locality and spatial locality.	3

PART D

Answer any two questions, each carries 9 marks

12	a)	Differentiate centralized and distributed bus arbitration mechanism used in DMA.	4
	b)	Give the structure of a typical static RAM cell and explain its read and write operations.	5

13 Differentiate serial port and parallel port. Draw the diagram of a bidirectional 8-bit parallel interface and explain its working. 9

14 Elaborate the various cache mapping techniques with an example for each. 9

PART E

Answer any four questions, each carries 10 marks

15 a) Write the Register Transfer Logic format for a conditional control statement. Give an example and explain the same. 4

b) Mention the advantages of using a scratch pad memory. Draw the diagram of a processor that employs a scratch pad memory and explain the same. 6

16 a) Design an adder/subtractor circuit with one selection variable *s* and two inputs *A* and *B*. When $s = 0$ the circuit performs $A + B$. When $s = 1$ the circuit performs $A - B$ by taking 2's complement of *B*. 5

b) Design a 4-bit combinational logic shifter with 2 control signals H_1 and H_0 that performs the following operations (bit values given in parenthesis are the values of control variables H_1 and H_0 respectively):- No shift (00), Shift-right (01), Shift-left (10), Transfer 0's to S (11). 5

17 a) Draw and explain the block diagram for a 4-bit complete accumulator 6

b) Discuss about condition code bits in a 4 bit status register 4

18 Design a hard-wired control unit based on the one flip-flop per state method to add/subtract 2 signed numbers represented in the sign-and-magnitude form. 10

19 Explain the organization of a microprogrammed computer with a block diagram 10

20 Draw a neat block diagram of a microprogram sequencer and explain its working. 10

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Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY
FOURTH SEMESTER B.TECH DEGREE EXAMINATION(S), DECEMBER 2019

Course Code: CS202

Course Name: COMPUTER ORGANISATION AND ARCHITECTURE

Max. Marks: 100 Duration: 3 Hours

PART A

Answer all questions, each carries 3 marks

1		Give the relevance of MAR, PC and IR in a typical computer system with neat diagram.	3
2		Differentiate between Big-endian and Little-endian assignment for word addressing.	3
3		Illustrate the advantages of using multiple bus organization over single bus organization with the help of a sample instruction execution.	3
4		Divide 25 by 8 using restoring division algorithm.	3

PART B

Answer any two questions, each carries 9 marks

5	a)	Define Addressing mode and explain Different types of addressing modes with an example for each.	6
	b)	Show the effect of stack operations on the stack with diagram.	3
6	a)	What is meant by instruction sequencing? Discuss the different types of instruction sequencing with example.	4
	b)	Illustrate Booth multiplication with an example	5
7	a)	Discuss the data path inside the processor with single bus organization with neat diagram	4
	b)	Write down the control sequence for the execution of the instruction *Add (R1), R2* in single bus organization	5

PART C

Answer all question, each carries 3 marks

8		Discuss the different ways of accessing I/O devices of a computer system.	3
9		Explain the daisy chain method with neat diagram	3
10		Justify the need of memory hierarchy in a computer and discuss the various parameters that are considered for the formation of memory hierarchy.	3
11		Discuss about different types of RAMs.	3

PART D

Answer any two questions, each carries 9 marks

12 a) What is interrupt? Discuss the differences between subroutine and interrupt service routine. 4

b) Describe the different bus arbitration techniques for DMA data transfer. 5

13 a) Explain semiconductor ROM memories 4

b) Discuss the SCSI protocol for a complete disk read operation by listing out the sequence of events involved in it. 5

14 a) How do you relate set associative mapped cache with Direct mapped and associative mapped cache mechanisms? 3

b) Design a 64K x 8 memory module using 16K x 1 static memory chips. 6

PART E

Answer any four questions, each carries 10 marks

15 a) Write short notes on Arithmetic , logic and shift microoperations with examples 6

b) Show the block diagram that executes the following conditional control statements

C' T_2 : F ← A 4

C T_2 : F ← B where C is the conditional variable and A, B , F are registers

16 Draw the block diagram of a processor unit with 16 selection variables and discuss the functions of selection variables. Derive the control word for the micro operation R1 ← R1 – R2. 10

17 Discuss the major operations that can be performed by a parallel adder in the design of arithmetic circuit. 10

18 Discuss the different methods of control logic design in detail 10

19 Describe the organization of micro program sequencer with neat diagram. Also provide its address sequencing capabilities. 10

20 Explain the horizontal and vertical microinstructions in microprogrammed control. 10

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Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

Fourth semester B.Tech examinations (S), September 2020

Course Code: CS202

Course Name: COMPUTER ORGANISATION AND ARCHITECTURE (CS, IT)

Max. Marks: 100 Duration: 3 Hours

PART A

Answer all questions, each carries 3 marks

1		What is meant by zero- address instruction?	(3)
2		Design 2×2 array multiplier.	(3)
3		Autoincrement mode is useful for accessing data items in successive memory locations. Justify the statement.	(3)
4		Draw the flowchart for Booth's Multiplication algorithm.	(3)

PART B

Answer any two questions, each carries 9 marks

5	a)	How the byte addresses are assigned across word?	(5)
	b)	Explain the execution of a complete instruction.	(4)
6	a)	Specify the actions needed to execute the instruction Move (R1), R2	(5)
	b)	What is the role of processor stack in subroutine call and return?	(4)
7	a)	Explain restoring method of division with the help of a flow chart.	(5)
	b)	Compare and contrast single bus and multiple bus organization of processor.	(4)

PART C

Answer all question, each carries 3 marks

8		What is the function of interrupt-service routine?	(3)
9		How the time involved in polling process is reduced in interrupted I/O?	(3)
10		Write notes on synchronous DRAM.	(3)
11		Illustrate LRU cache replacement algorithm.	(3)

PART D

Answer any two questions, each carries 9 marks

12	a)	Differentiate the data transfer in programmed I/O and interrupt driven I/O	(5)
	b)	Write about the DMA controller registers that are accessed by the processor to initiate data transfer.	(4)

13	a)	Differentiate between associative mapping and set associative mapping.	(5)
	b)	Illustrate the operation of the Small Computer System Interface bus.	(4)
14	a)	Describe different types of ROM	(5)
	b)	A computer system uses 32-bit memory addresses and it has a main memory consisting of 1G bytes. It has a 4K-byte cache organized in the set-associative manner, with 4 blocks per set and 64 bytes per block. Calculate the number of bits in each of the Tag, Set, and Word fields of the main memory address.	(4)

PART E

Answer any four questions, each carries 10 marks

15	a)	What are conditional control statements? Represent the following conditional control statement by two register transfer statements with control functions. $If\,(P=1)\ then\,(R1 \leftarrow R2)\ \ else\ if\ (Q=1)\ then\,(R1 \leftarrow R3)$	4
	b)	Write notes on status register	6
16	a)	Explain horizontal and vertical micro instructions, with suitable examples.	5
	b)	Explain how control signals are generated in one flip flop per state control logic with the help of a diagram	5
17		Outline the organisation of a full processor unit showing the control inputs to all components. Show with the help of an example, how an instruction is implemented by giving necessary control inputs to different parts of the processor.	10
18		Illustrate the basic arithmetic microoperations in a 4 bit ALU with the help of a parallel adder.	10
19		Explain with the help of an example how control signals are generated using hardwired control.	10
20		Describe the purpose of microprogram sequencing. How is it carried out?	10

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