

Reg. No. \_\_\_\_\_ Name: \_\_\_\_\_

**APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY**  
**FOURTH SEMESTER B.TECH DEGREE EXAMINATION, JUNE 2017**

Course Code: **EC206**

Course Name: **COMPUTER ORGANISATION (EC)**

Max. Marks: 100

Duration: 3 Hours

### PART A

***Question No.1 is compulsory. Answer either Question No. 2 or Question No. 3.***

1. (a) Illustrate the basic functional units of a digital computer and list the important functions of each unit. (4)
- (b) Explain briefly the principle of carry look-ahead addition. Draw the circuit diagram of 4 bit carry look-ahead adder with proper design. (7)
- (c) With the help of suitable examples, differentiate between R-type and I-type instructions in MIPS machine language. (4)
2. (a) Illustrate the IEEE standard format for single precision floating point numbers. (2)
- (b) Compute the delay of a 64-bit carry prefix adder, assuming that each 2-input gate delay is 200 ps. (4)
- (c) With a suitable circuit arrangement, explain n-bit binary multiplication. (6)
- (d) Design and implement a 4-bit equality comparator using gates. (3)
3. (a) Illustrate the format of J-type instructions in MIPS machine language. (2)
- (b) Write short notes on (i) MIPS register set (ii) Byte addressable memory. (7)
- (c) Assuming that the opcode 'addi' is represented by  $8_{10}$ , register 'add' operation is represented by the function code  $32_{10}$ , and the registers  $s_0$  to  $s_7$  are represented by  $16_{10}$  to  $23_{10}$  in MIPS machine language,
  - (i) Translate the following machine language code into MIPS assembly language:  $0x2237FFF3$  (3)
  - (ii) Translate the following MIPS assembly code to MIPS machine language code in hexadecimal form: `add $s0, $s4, $s5` (3)

### PART B

***Question No.4 is compulsory. Answer either Question No. 5 or Question No. 6.***

4. (a) With examples for each, explain the addressing modes available in MIPS. (7.5)

- (b) What is micro architecture? List the state elements of MIPS processor and their functions. (5)
- (c) Write a short note on performance analysis of computer systems. (2.5)
5. (a) With an illustration, briefly explain MIPS memory map. (5)
- (b) With a suitable diagram, explain the steps involved in executing a high level language program. (6)
- (c) With an example, briefly explain pseudo instructions in MIPS. (4)
6. (a) Differentiate between the three micro architectures for MIPS processor architecture. (3)
- (b) Derive the simplified expression for cycle time in a single cycle MIPS processor. If the cycle time in a single cycle processor is 1000 ps, compute the total execution time (in seconds) for a program with 10 lakh instructions. (7)
- (c) List the three main weaknesses of a single cycle processor. How are they eliminated in a multi cycle processor? (5)

**PART C**

***Question No. 7 is compulsory. Answer either Question No. 8 or Question No. 9.***

7. (a) With the help of a diagram, explain the concept of memory hierarchy. (4)
- (b) Write short notes on (i) SCSI (ii) USB (6)
- (c) With a diagram, explain address translation in virtual memory. (7)
- (d) Differentiate between the two different write policies in cache memory. (3)
8. (a) Explain in detail, the different modes of data transfer between the processor/memory and I/O devices in a computer system. (10)
- (b) What is a port? Differentiate between serial and parallel ports. (4)
- (c) With a circuit diagram, explain the working of a DRAM cell. (6)
9. (a) Briefly explain the concept of cache memory. What is hit rate? (3)
- (b) Discuss in detail, any two mapping methods in cache memory. (12)
- (c) Write short notes on (i) Replacement algorithms (ii) TLB (5)

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**APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY**  
**FOURTH SEMESTER B.TECH DEGREE EXAMINATION, JULY 2017**

**Course Code: EC206**

**Course Name: COMPUTER ORGANISATION (EC)**

Max. Marks: 100

Duration: 3 Hours

**PART A**

*Question No.1 is compulsory. Answer question 2 or 3. Each carries 15 marks.*

- 1 a) Design a multiplier to multiply two 4-bit numbers. Illustrate with an example. (8)
- b) Convert the following MIPS assembly code into machine language. Write the instructions in hexadecimal. (7)
 

```
addi $s0, $0, 73
sw $t1, -7($t2)
sub $t1, $s7, $s2
```
- 2 a) Design a shifter that always shifts a 32 bit input left by 2 bits. The input and output are both 32 bits. Explain the design and sketch a schematic. (6)
- b) Show the schematic of a sign extension unit with a 4-bit input and an 8-bit output. (4)
- c) Express the following base 10 numbers in IEEE 754 single precision floating-point format: (5)
 

(i) -13.5625            (ii) 42.3125

**OR**

- 3 a) Differentiate Big-Endian and Little-Endian machines. (3)
- b) Explain the various instruction formats of MIPS with examples. (7)
- c) Give a brief account of the architecture of MIPS. (5)

**PART B**

*Question No.4 is compulsory. Answer question 5 or 6. Each carries 15 marks.*

- 4 a) Explain any three state elements of a MIPS processor. (5)
- b) What is an exception? How exceptions are classified and handled? (7)
- c) Mention any three advantages of multi cycle implementation compared to single cycle implementation. (3)
- 5 a) Explain various addressing modes of MIPS with examples. (10)
- b) What is the range of instruction addresses to which conditional branches such as **beq** and **bne** can branch in MIPS? Give your answer in number of instructions relative to the conditional branch instructions. (5)

**OR**

- 6 a) Draw the data path for single cycle processor for R-type instruction along with the control signals. Explain the design procedure for the control unit. (9)
- b) Draw the datapath for multicycle processor for R-type instruction and explain (6)

**PART C**

*Question No.7 is compulsory. Answer question 8 or 9. Each carries 20 marks.*

- 7 a) Briefly explain the standard I/O interfaces:- (10)  
(i) Serial port (ii) Parallel port (iii) USB.
- b) Explain clearly the address translation mechanism in virtual memory. (10)
- 8 a) Draw the internal organization of a SRAM cell and explain the read and write operation. (10)
- b) Explain DMA data transfer method. What are the advantages of DMA transfer? (10)

**OR**

- 9 a) Explain direct mapped cache structure. (8)
- b) Here is a series of address references given as word addresses: (12)  
1,4,8,5,20,17,19,56,9,11,4,43,5,6,9,17.

Assuming a direct mapped cache with 16 one-word blocks that is initially empty, label each reference in the list as a hit or a miss and show the final contents of the cache.

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**APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY**  
**FOURTH SEMESTER B.TECH DEGREE EXAMINATION, APRIL 2018**

**Course Code: EC206**

**Course Name: COMPUTER ORGANISATION (EC)**

Max. Marks: 100

Duration: 3 Hours

**PART A**

*Answer any two full questions, each carries 15 marks*

Marks

- |   |   |     |
|---|---|-----|
| 1 | a) Express $(-18.125)_{10}$ in IEEE 754 single-precision floating point format.   | (3) |
|   | b) What is the use of a carry propagate adder? Design a 32-bit carry propagate adder.   | (5) |
|   | c) What are the 4 design principles of MIPS architecture? Explain   | (7) |
| 2 | a) Design a 3-bit equality comparator   | (3) |
|   | b) Design and implement hardware for a 4-bit logical shift right circuit.   | (4) |
|   | c) List out the functions performed by an ALU. Design an ALU using adder, inverter, multiplexer blocks and basic digital gates. | (8) |
| 3 | a) List the 3 MIPS instruction formats with examples.   | (3) |
|   | b) With a diagram explain the R-type machine instruction format   | (5) |
|   | c) With a diagram explain the R-type machine instruction format   | (7) |
- Translate the following I-type assembly instruction into machine code.  
*lw \$s3, -24(\$s4)*. Write the instruction in hexadecimal.  
 Hint: [*\$s3* and *\$s4* are registers 19 and 20, respectively.]

[*lw* has an opcode of 35.]

**PART B**

*Answer any two full questions, each carries 15 marks*

- |   |   |      |
|---|---|------|
| 4 | a) What are the different processes required to translate a program from a high-level language into machine language and executing it? Explain. | (7)  |
|   | b) What are the 3 state elements of multi cycle MIPS processor? Explain each with diagram   | (8)  |
| 5 | a) Define Pseudo instruction and write MIPS instruction for the following pseudo instructions   | (5)  |
|   | i) clear \$t0                      ii) nop  |      |
|   | b) Explain about the different addressing modes in MIPS.  | (10) |
| 6 | a) Draw datapath for single cycle implementation for R-type instructions along with   | (10) |

central signals. Explain clearly.

- b) What are the 3 advantages of multi cycle processor over single cycle processor? (5)

### PART C

*Answer any two full questions, each carries 20 marks*

- 7 a) Define Miss Rate, Hit Rate and Average memory access time. (6)  
b) What is meant by ROM? Explain the various types of ROM. (4)  
c) Explain with a diagram how virtual memory address is translated to physical address using page table. (10)
- 8 a) Explain the working of DRAM and SRAM with neat diagram. (10)  
b) Explain the various data transfer methods. (10)
- 9 a) Explain direct mapping in cache memory with diagram. (8)  
b) What are the write policy classifications of cache memory? Explain. (6)  
c) What is the role of TLB (Translation Look aside Buffer) in virtual address translation? (6)

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**APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY**  
 FOURTH SEMESTER B.TECH DEGREE EXAMINATION, DECEMBER 2018

**Course Code: EC 206**

**Course Name: COMPUTER ORGANIZATION**

Max. Marks: 100

Duration: 3 Hours

**PART A (MODULE I & II)**

*Answer any two out of three questions*

Marks

- 1 (a) How is Carry- Look ahead Adder different from Ripple Carry Adder? Explain (10)  
with relevant diagrams and write down the delay equations for both adders.
- b In a 32- bit Adder circuit assume each 2 -input gate delay is 200ps. Calculate (5)  
(a) Total delay for a Carry Look Ahead adder when the full adder delay is 400ps  
and is divided in to 4 bits block (b) Total delay for a Prefix Adder.
- 2 a Design a 16-bit prefix adder and explain its working. Also obtain the delay of an (10)  
N-bit prefix adder
- b What is meant by R-Type instruction? Draw the R-Type machine instruction (5)  
format. Find the machine code for the R-Type instruction add  $Rs0, Rs1, Rs2$  with  
function code 32.
- 3 a Design a 4-bit right and left shifter using multiplexers. (5)
- b What are I-Type instructions ? Explain with its instruction format. (5)
- c Explain the MIPS assembly codes for conditional branch instructions *beq* and *bne* (5)  
with examples.

**PART B (MODULE III&IV)**

*Answer any two out of three questions.*

- 4 a Discuss the different MIPS addressing modes. (8)
- b What are Pseudo instructions? Given the pseudo instruction " mov \$s1,\$s2 ". (7)  
Write down its corresponding MIPS instruction and explain its working.
- 5 a Describe step by step the working of a single cycle data path for subtracting two (10)  
numbers.
- b What are the parameters used for the performance analysis of a single cycle (5)  
processor? Explain.

- 6 a Draw and explain the working of complete MIPS multi cycle processor using an example. (10)
- b What are the steps involved in translating a high level language program into a machine language program ? (5)

**PART C(MODULE V&VI)**

*Answer any two out of three questions. Each carries 20 marks*

- 7 a A program has 2000 data access instructions (loads or stores), and 1250 of these requested data values are found in the cache. The other 750 data values are supplied to the processor by main memory or disk memory. What are the miss and hit rates for the cache? (5)
- b What is virtual memory ? Explain the process of address translation. (5)
- c Differentiate between programmed I/O and interrupt driven I/O. (5)
- d How is SRAM different from DRAM? (5)
- 8 a Explain the principle of Cache memory. What are the different cache mapping techniques? Discuss in detail. (10)
- b What is page table and how is it useful in address translation? (5)
- c Explain DMA. (5)
- 9 a Why standardisation of input/output interfaces is necessary? Explain PCI, SCSI and USB. (8)
- b Explain the memory system hierarchy. Draw and explain the internal organization of a memory chip. (7)
- c What are the various write policies used in cache? (5)

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**APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY**  
**FOURTH SEMESTER B.TECH DEGREE EXAMINATION(R&S) MAY 2019**

**Course Code: EC206**

**Course Name: COMPUTER ORGANISATION (EC)**

Max. Marks: 100

Duration: 3 Hours

**PART A**

*Answer any two full questions, each carries 15 marks*

Marks

- |   |   |     |
|---|---|-----|
| 1 | a) Explain Propagate adder and ripple carry adder.  | (8) |
|   | b) Illustrate the use of shifters and rotators with example in arithmetic circuits.       | (7) |
| 2 | a) Define the following terms of MIPS processor:  | (8) |
|   | (i) Register Set. (ii) Operands. (iii) Memory. (iv) Registers.                            |     |
|   | b) With example explain briefly R-type and I-type Instruction format in Machine Language. | (7) |
| 3 | a) Define fixed point number systems with examples.                                       | (7) |
|   | b) Convert to MIPS assembly instruction (i) 0x2128FF6A                                    | (8) |
|   | (ii) 0x0253882A   |     |

**PART B**

*Answer any two full questions, each carries 15 marks*

- |   |  |     |
|---|--|-----|
| 4 | a) Explain Pseudoinstructions and exceptions in MIPS.                    | (8) |
|   | b) Explain Floating Point instructions used in MIPS                      | (7) |
| 5 | a) Briefly define the state elements used in MIPS processor.             | (7) |
|   | b) Explain the data path of single cycle R-type instruction.             | (8) |
| 6 | a) With neat diagram explain multi cycle control for R-type instruction. | (8) |
|   | b) Explain signed and unsigned instructions used in MIPS                 | (7) |

**PART C**

*Answer any two full questions, each carries 20 marks*

- 7 a) Illustrate the different modes of data transfer in I/O systems. (5)  
b) Mention the working of memory cells SRAM and DRAM. (10)  
c) Draw Memory Hierarchy diagram. (5)
- 8 a) Explain Address Translation in virtual Memory. (8)  
b) With neat diagram explain briefly TLB. (7)  
c) Define Write through and Write Back Policies. (5)
- 9 a) Illustrate the different mapping methods of Cache Memory. (8)  
b) Write short notes on Segmentation and paging. (7)  
c) Sketch the internal organization of a memory chip. (5)

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**APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY**  
FOURTH SEMESTER B.TECH DEGREE EXAMINATION(S), DECEMBER 2019

**Course Code: EC206**

**Course Name: COMPUTER ORGANISATION**

Max. Marks: 100

Duration: 3 Hours

**PART A**

*Answer any two full questions, each carries 15 marks*

Marks

- |   |  |     |
|---|--|-----|
| 1 | a) Explain with neat diagram a 32 bit ripple carry adder.  | (3) |
|   | b) With neat diagram explain Arithmetic Logic Unit   | (5) |
|   | c) Explain the R- type instruction format of MIPS with example   | (3) |
|   | d) Translate the following machine language code into MIPS assembly language:<br>0xAD310004                        | (4) |
| 2 | a) Design a 4×4 binary multiplier. Illustrate with an example  | (7) |
|   | b) Write notes on MIPS register set.   | (4) |
|   | c) Translate the following MIPS assembly code to MIPS machine language code in hexadecimal form: lw \$t2, 32 (\$0) | (4) |
| 3 | a) Explain how floating point numbers are represented in computer's memory.  | (6) |
|   | b) Differentiate Big-Endian and Little-Endian machines   | (4) |
|   | c) Explain load word and store word instructions with examples   | (5) |

**PART B**

*Answer any two full questions, each carries 15 marks*

- |   |   |      |
|---|---|------|
| 4 | a) With examples, explain the different addressing modes available in MIPS.                                 | (10) |
|   | b) Explain the control unit of a multi cycle processor  | (5)  |
| 5 | a) Explain the various steps for executing a program  | (9)  |
|   | b) What are the weaknesses of a single cycle processor. How are they eliminated in a multi cycle processor? | (6)  |
| 6 | a) What are exceptions ? How the exceptions are handled ?   | (7)  |
|   | b) Draw and explain datapath for single cycle implementation for R-type instructions.                       | (8)  |

**PART C**

*Answer any two full questions, each carries 20 marks*

- |   |  |      |
|---|--|------|
| 7 | a) With the help of a diagram, explain the concept of memory hierarchy.                                    | (5)  |
|   | b) Distinguish between Programmed I/O and Interrupt driven I/O   | (5)  |
|   | c) Explain how a virtual address is translated into a physical address in virtual memory using page table. | (10) |
| 8 | a) Differentiate between SRAM and DRAM   | (6)  |

- b) Write short notes on (i) Serial port (ii) Parallel port (4)
- c) Explain LRU replacement algorithm (4)
- d) Explain with diagram direct mapping method in cache memory. (6)
- 9 a) What is meant by ROM? Explain the various types of ROM (5)
- b) With the help of a circuit diagram, explain the working of a SRAM cell. (5)
- c) Explain the concept of cache memory. Also define Miss Rate, Hit Rate and Average memory access time. (10)

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Reg No.: \_\_\_\_\_

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**APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY**

Fourth semester B.Tech examinations (S), September 2020

**Course Code: EC206****Course Name: COMPUTER ORGANISATION (EC)**

Max. Marks: 100

Duration: 3 Hours

**PART A***Answer any two full questions, each carries 15 marks*

Marks

- 1 a) Draw the block diagram of a 16-bit ripple carry adder using full adders. Calculate the delay of a 32-bit ripple carry adder. Assume a full adder delay is 200ps. (7)
- b) Express the following base 10 numbers in 16-bit fixed-point two's complement format with eight integer bits and eight fraction bits. Express in IEEE 754 single-precision floating-point format also. Express your answer in hexadecimal. (8)
- (a) -20.5 (b) 24.25
- 2 a) Explain any two assembly instruction formats in MIPS with examples. (6)
- b) Write the operation performed in MIPS processor when it executes the following instructions (9)
- (a) add \$t0, \$s4, \$s5  
(b) lw \$t2, 32(\$0)  
(c) sw \$s1, 4(\$t1)
- 3 a) Draw the symbol and implementation of a 4 x 4 multiplier. (7)
- b) Discuss about operands and registers of MIPS processor. Write the use of \$0, \$gp, \$sp and \$t8. (8)

**PART B***Answer any two full questions, each carries 15 marks*

- 4 a) Explain five addressing modes of MIPS with example. (15)
- 5 a) Draw the datapath for single cycle processor for *sw* instruction. (9)
- b) List the characteristics of single-cycle and multi cycle microarchitectures. (6)
- 6 a) How does a multicycle processor address the weakness of single-cycle processor? (7)
- b) Explain the steps involved in executing a high level language program. Draw the flow chart. (8)

**PART C**

*Answer any two full questions, each carries 20 marks*

- 7 a) Explain any two modes of data transfer between the processor/memory and I/O devices in a computer system. (6)
- b) Draw the internal organization of a DRAM cell and explain the read and write operation. (6)
- c) Illustrate virtual address to physical address translation using page table. (8)
- 8 a) Define miss rate and average memory access time. (6)
- b) Draw the internal organization of a SRAM cell and explain the read and write operation. (8)
- c) Compute the size of a 4096-word x 32-bit memory array. Also find the width of address and data bus. (6)
- 9 a) Describe temporal locality and spatial locality with respect to cache memory. (6)
- b) Illustrate how data is found in a C=8 word, 2-way set associative cache (10)
- c) Draw the internal organization of a 4 x 3 memory array. (4)

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